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Book Two

Instruction Manual
for

ANDS5400

Modular A/D and D/A Data Acquisition & Distribution Systems with Digital I/O Capability

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9
INTRODUCTION

Book Two, providing the technical data necessary to document the user cards in any data acquisition/data distribution application, is conveniently divided into six chapters: "Analog Multiplexers," "D/A Converters," "Digital Input," "Digital Output," "Self-Test Card," and "I/O Cables." The functional versatility offered by over 80 input/output devices is the key feature of the ANDS5400 system; furthermore, since Analogic is continually evolving and increasing the library of user cards, the opportunity for expansion with this flexible data acquisition/data distribution system is virtually limitless. However, to optimize the performance of the ANDS5400 and its user cards, the customer must be thoroughly familiar with the operation of the master and expansion chassis explained in Book One.

For a particular application the customer can choose from several user cards described in each chapter. At the beginning of each chapter is an index of the data sheets, schematics, and drawings in that chapter. For each user card there is a general description, a block diagram, specifications, a theory of operation, and schematics. The "Analog Multiplexers" chapter includes data on a range of sample-and-hold amplifiers, isoplexers, isolation amplifiers, and high level filter multiplexer cards. The "Analog Output" chapter describes several D/A converters. An important feature of the "Digital Input" chapter is a detailed analysis of the digital input interrupt structure with programming examples; this interrupt scheme allows a priority system to be established with most configurations. The next chapter contains technical data on a variety of output cards, and the "Self-Test Card" chapter describes the diagnostic card. Book Two concludes with a set of schematics for I/O cable assemblies available for the user cards.

Note: Table 9-1 in this "Introduction" provides power consumption data on individual user cards.

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Table 9-1 User Card Power Consumption*

Card Type	+5V	+15V	−15V	Comments
AC405X	<10mA	30mA	30mA	
AC407X	300mA	30mA	30mA	
AC425X	<20mA	30mA	30mA	
AC427X	300mA	30mA	30mA	
AC43XX	300mA	25mA	25mA	(External Excitation)
AC43XX	300mA	355mA	355mA	(Worst Case. Maximum Bridge Current Internal Excitation)
AC47XX	20mA	30mA	30mA	
AC280	50mA	60mA	60mA	
AC281	50mA	150mA	100mA	
AC133X	40mA	125mA	150mA	
AC153X	40mA	40mA	80mA	
AC1562	60mA	65mA	140mA	
AC17XX	700mA	200mA		(200mA May Be From + Or - 15V)
AC18XX	120mA	120mA	120mA	
AC19XX	220mA	190mA	60mA	(+15V Is 50mA On Non-TC Versions)
DC6000	200mA			(No ISO's, No Connections)
DC61X0	200mA			
DC62XX	340mA			(With ISO's, No Connections)
DC63XX	350mA			
DC6510	350mA			
DC66XX	150mA			(With ISO's, No Connections)
DC6700	400mA			
DC6701	50mA			(External Coil Power)
DC6702	50mA			(External Coil Power)
DC6710	600mA			
DC6711	50mA			(External Coil Power)
DC6712	50mA			(External Coil Power)
AC30X0	20mA	40mA	150mA	(150mA Tapers Off To 75mA After Warm-up)

* For more information refer to the "Power Consumption Characteristics" section in the "Introduction" chapter of Book One.

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Analog Multiplexers

Card Number	Drawing Number	Title
AC280/AC281	—	AC280/AC281 Simultaneous Sample-and Hold Data Sheet
MP240 & MP240-1	—	MP240 & MP240-1 S&H Amplifiers Data Sheet
MP270	—	MP270 S&H Amplifier Data Sheet
AC280/AC281	C5-7440	AC280/AC281 4 Channel SSH Schematic
AC280	D7-7440	AC280 4 Channel SSH Assembly
AC4050	—	AC4050 Series Isoplexer Data Sheet
AC4250	—	AC4250 Series Thermoplexer Data Sheet
MP225A	—	MP225A Isolation Amplifier and MP235 Driver Data Sheet
MP226	—	MP226 Isolation Amplifier and MP235 Driver Data Sheet
AC4050 to AC4060/ AC4250 to AC4256	D5-8632	AC4050 to AC4054 / AC4250 to AC4256 Isoplexer/Thermoplexer Schematic
AC4050 to AC4060/ AC4250 to AC4256	D7-8632	Isoplexer/Thermoplexer Card Assembly
AC4300	—	Bridge Transducer Input Card Data Sheet
MP227	—	Isolation Amplifier Data Sheet
AC43XX	D5-8668	AC43XX Bridge Completion (Strain Gauge) Card Schematic
AC43XX	D7-8668	AC43XX Bridge Completion (Strain Gauge) Card Assembly
AC4380	D7-8672	AC4380 Bridge Completion (Strain Gauge) Board
AC4720	—	AC4720 High Level Single-Ended/Differential Multiplexer Data Sheet
AC4730	—	AC4730 Series High Level Filter Multiplexer Data Sheet
AC4740	—	AC4740 Differential Input Current (0-50mA) Multiplexer Data Sheet
AC4750	—	AC4750 High Level Attenuator Multiplexer Data Sheet
AC47XX	D5-7437	AC47XX 32 Channel Signal Conditioner — Mux Schematic
AC47XX	D7-7437	AC47XX 32 Channel Signal Conditioner — Mux Assembly

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AC280/AC281

SIMULTANEOUS SAMPLE & HOLD FOR ANDS5400

GENERAL DESCRIPTION

The AC280 and the AC281 are simultaneous sample-and-hold input cards, each containing four sample and hold amplifiers together with the necessary digital control and analog multiplexing circuitry required for operating and interrogating the sample-and-hold circuits.

The AC280 is a moderate speed card while the AC281 is a high speed version suitable for fast moving signals. Optionally, (consult factory) either card may be ordered with special input conditioning circuitry. Available input circuit options include overvoltage protection (up to ±200Vdc), high impedance inputs (10^{11} ohms), single-ended inputs with gain, differential inputs, differential inputs with gain, and single-pole input filter capability.

The purpose of these devices is to acquire analog signals and simultaneously hold them for processing. The sample-and-hold channels are rapidly scanned by high speed multiplexing techniques. The resulting data represents the analog signal in digital format with minimum time skew between channels.

SPECIFICATIONS

	AC280	AC281
Input Voltage max.	± 10.3V	± 10.3V
Max. Input without Damage	± 15V	± 15V
Slew Rate	5V/μs	50V/μs
Input Impedance	10^8 ohms	10^8 ohms
Input Capacitance	20pF	20pF
Acquisition Time (20V Step)	7μs	1.3μs
Noise (p-p)	300μV	300μV
Sample-to-Hold Settling	2μs	0.7μs
Transfer Accuracy	0.01% FSR	0.01% FSR
Droop Rate	1μV/μs	2μV/μs
Offset Error	Adjustable to zero	Adjustable to zero

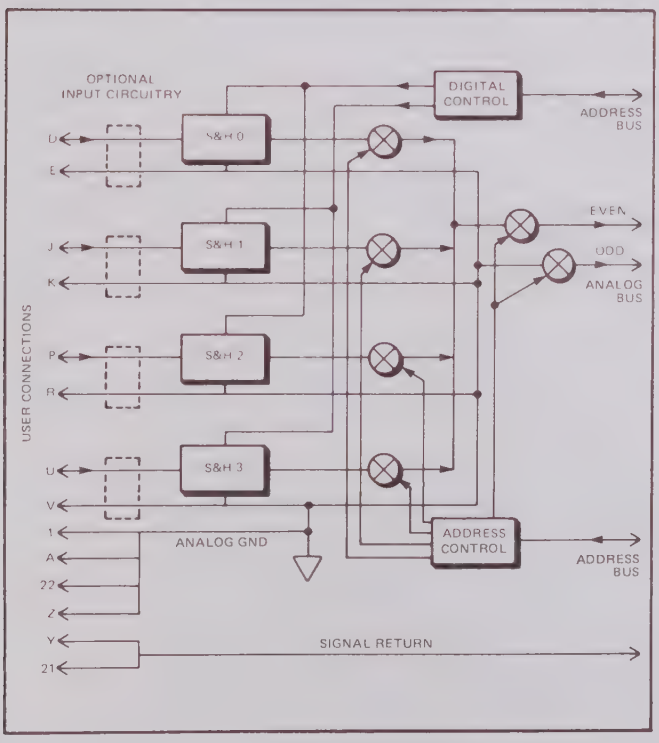

Fig.1. AC280/AC281 SS&H simplified block diagram.

OPERATION

When installed in the ANDS5400 System, the AC280 and AC281 are controlled by the standard command structure for simultaneous sample-and-hold cards. To operate the cards, the following conditions must be set up by the interface:

Digital Address Decoding: "OUT" Mode

For each function to be performed, the address register is loaded with the appropriate address, and a "Dig Out" pulse is applied. The function will then be carried out by all simultaneous sample-and-hold cards in the system.

ADDRESS	*FUNCTION*
4000	All Channels in "Sample"
4001	Channels 0 & 2 in "Hold" (Even)
4002	Channels 1 & 3 in "Hold" (Odd)
4003	All Channels in "Hold"

The routine described above may be carried out by direct manipulation of the appropriate lines with the zero level interface or by using OP Code 11 with the General Purpose Interface. When using the General Purpose Interface, the data applied with the second part of OP Code 11 is ignored.

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To use an external signal to control the synchronization of the sample-and-hold cards, a similar procedure is used with the following addresses.

ADDRESS	*FUNCTION*
6000	All Channels in "Sample"
6001	Channels 0 & 2 in "Hold" (Even)
6002	Channels 1 & 3 in "Hold" (Odd)
6003	All Channels in "Hold"

When using the "4000" series addresses, the functions will be carried out immediately. However, when using the "6000" series addresses, the functions will be carried out after the hold line from J28 on the rear panel of the ANDS5400 has been raised to a logical "1", thus providing external timing control over the sample-and-hold operation (see AN5400 Manual).

Applying a "clear" command through any ANDS5400 interface will immediately cause all sample-and-holds to enter the "sample" mode.

Measurement of the four channels is done in the manner used for any analog input channel. While in the "hold" mode, the sample-and-hold outputs are referenced to analog ground as shown in the block diagram (Fig. 1). Since Analog ground is a power supply return, there is likely to be current flowing that would cause a ground voltage drop between the sample-and-hold card and the A/D converter. To prevent errors caused by this ground drop, the output multiplexing on the card has been configured to allow differential measurements between the sample-and-hold output and the local analog ground on the sample-and-hold card. Thus, when measuring the sample-and-hold outputs, the octal range code used should be 10, 11, 12, or 13 depending on the desired gain (See Signal Processor, AN5400 Data Sheet Book).

CALIBRATION

Located along the top edge of the AC280 and AC281 cards are four potentiometers labeled CH 0, 1, 2, and 3. These controls are used to remove the offset errors from each sample-and-hold. Two procedures are offered for adjusting these offset potentiometers should calibration prove necessary. The first procedure is a simple one that can be performed under local control, while the second procedure is slightly more accurate, but requires a remotely operated computer program.

Local Control

Connect shorting jumpers across the inputs of each sample-and-hold. (i.e., D-E, J-K, P-R, U-V). Apply the "4000" code as an out address to place the sample and holds in "sample". Apply the appropriate input address for the first channel and apply range code 10. Observe the A/D output data and adjust the CH 0 pot until the code representing zero voltage is solidly displayed. Address and adjust the remaining channels.

Computer Control

This procedure is slightly more accurate because it will account for the sample-and-hold "pedestal" which is a small (15mV or less) offset that occurs when switching from sample to hold.

Install the input shorting jumpers as before. Generate a short computer program that will place the sample and hold amplifiers in sample for about a millisecond, then switch them to hold, measure the output, and return to sample. Adjust the appropriate potentiometers to obtain the zero code as measured for each amplifier.

ADDRESSING

The address structure of the ANDS5400 provides complete flexibility of configuration and installation. Table 1 details the addresses of devices installed in any enclosure. To determine the absolute address of this device, simply add to the address, listed in Table 1, the enclosure address in the Analog Mode (see ANDS5400 Manual). Note that the SSH control functions i.e., 4000, 6000, are implemented using Digital Mode addressing.

Table 1

Address Locations (Octal)

J1	0,	10,	20,	30	J9	400,	410,	420,	430
J2	40,	50,	60,	70	J10	440,	450,	460,	470
J3	100,	110,	120,	130	J11	500,	510,	520,	530
J4	140,	150,	160,	170	J12	540,	550,	560,	570
J5	200,	210,	220,	230	J13	600,	610,	620,	630
J6	240,	250,	260,	270	J14	640,	650,	660,	670
J7	300,	310,	320,	330	J15	700,	710,	720,	730
J8	340,	350,	360,	370	J16	740,	750,	760,	770

A Note About Dielectric Absorption

Dielectric Absorption causes a decay of the hold voltage on the hold capacitor due to the charge redistribution within the capacitor dielectric. This effect can cause an error when the hold capacitor is rapidly charged, then disconnected from the charging source. The following equation may be used to calculate the error for the AC280 or AC281. Note that the error increases with elapsed "Hold" time. It is therefore imperative, when using the SSH, to service it immediately when it is switched to "Hold".

$$\triangle E = E_S (1.5 \times 10^{-4}) \log_{10}\left(\frac{T_S + T_H}{T_S}\right)$$

where: $\triangle E$ = Error

E_S = Capacitor voltage change
T_S = Sample Time
T_H = Hold Time

Example: For a 20V Step, a sample time of 7μsec, and a hold time of 40μsec, $\triangle E = 2.5$mV.

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MP240 & MP240-1

High Performance, Low Cost General Purpose

SAMPLE & HOLD AMPLIFIERS

DESCRIPTION

The Analogic MP240 and MP240-1 Sample and Hold Amplifiers provide exceptional performance never before available in this price range. The MP240s feature a low aperture uncertainty (jitter of ±1ns), high transfer accuracy (within ±0.01% FSR), extremely low signal feedthrough in the Hold mode (–80dB), and a fast acquisition time (7μs and 5μs, respectively, to acquire a 20-volt step within 0.01%). Many of these high-performance features, previously available only in higher priced units, have been attained at reduced cost by using Analogic proprietary and proven circuit innovations, all in a low-profile (0.375"), fully shielded, metal case.

PERFORMANCE

The Analogic MP240 and MP240-1 Sample and Hold Amplifiers are complete units. As shown in Figure 1, they contain a high-impedance input buffer for minimum loading of analog signal sources, TTL/DTL/CMOS-compatible switching control for interfacing with any standard computer or digital control logic sources, and proprietary signal-guarded and signal-compensated acquisition and disconnect switching circuits for high performance accuracy. A high-quality holding capacitor for low droop rate and low dielectric absorption is included to maintain specified accuracy even at low conversion rates. The high-speed low-impedance output buffer is suitable for wideband system applications, and internally mounted high quality power supply bypass capacitors minimize the effects of power supply transients. Furthermore, these units provide the capability for external trimming to accommodate system offsets.

APPLICATION

The Analogic MP240s are especially useful for economical, high quality, wide-band signal data acquisition systems with throughput speeds up to 20kHz. For example, a low-cost, 16-channel, 12-bit analog data acquisition and conversion system can be assembled using the MP240 in combination with the Analogic MN4708 Multiplexer and the Analogic MP2412 Analog-to-Digital Converter. The Analogic AN3005 (115V AC input) or MP3020 (+5V DC input) power supply should be used if direct system powering is not readily available.

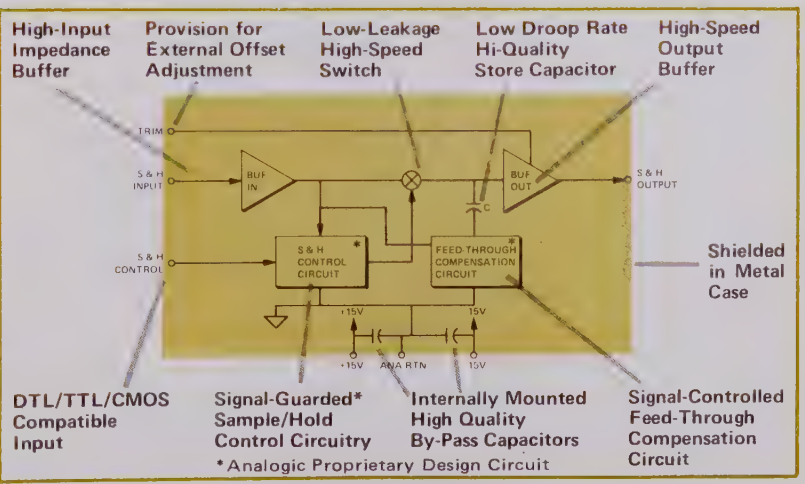

Figure 1. MP240 and MP240-1 Simplified Block Diagram and Performance Features

MAXIMIZED PERFORMANCE-TO-COST FEATURES

- High Transfer Accuracy ±0.01%
- Low Aperture Uncertainty <1ns jitter
- Exceptionally Low Signal Feedthrough –80dB
- Low Droop Rate <1μV/μs
- Low Noise <300μV p-p
- Fast Acquisition <5μs to 0.01% of 20-volt step (MP240-1)
- DTL/TTL/CMOS Compatible

APPLICATIONS

- Low-cost multi-channel simultaneous Sample and Hold Systems
- Wideband analog signal data processing systems
- Multi-channel D/A Sample and Hold Systems
- Telemetry demultiplexing systems

NOTE: Consult factory or nearest Analogic Representative for applications data concerning compatible A/D converters.

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MP240 & MP240-1 SPECIFICATIONS

SAMPLE MODE	
Input Voltage	±10V max. useful signal; ±15V max. without damage
Small Signal Bandwidth	300kHz
Full Power (±F.S.) Bandwidth	80kHz
Slew Rate	>5V/μs
Input Impedance	10^8 ohms in parallel with 10pF
Linearity	±0.005% FSR
Settling Time	MP240 5μs to 0.01% for 10V step 7μs to 0.01% for 20V step MP240-1 5μs to 0.01% for 20V step
Input Bias Current	<10nA
Noise	300μV peak-to-peak (3σ)
SAMPLE-TO-HOLD SWITCHING	
Aperture Time Uncertainty	±1 ns
Aperture Time	10ns typical, 20ns max.
Switching Transient Settling Time	<2μs
HOLD MODE	
Transfer Accuracy	±0.01% FSR (Gain = 1)
Droop Rate	<1μV/μs
Signal Voltage Feedthrough	−80dB
Offset	±10mV (adjustable to zero)
Offset Pedestal Uncertainty	<0.01% FSR
Offset Tempco	50μV/°C
Power Supply Sensitivity	0.0015%/%
OUTPUT	
Voltage	±10V
Max. Load	2kΩ in parallel with 200pF
Impedance	<1Ω
HOLD-TO-SAMPLE SWITCHING	
Acquisition Time	Same as settling time, above
SAMPLE & HOLD DIGITAL CONTROL	
Compatibility	DTL/TTL/CMOS compatible; 2 TTL loads
Sample	Logic "0", <0.4V
Hold	Logic "1", >3.0V
Required Rise Time	<10ns for specified Aperture Uncertainty
POWER SUPPLY	
+15V ±3%	20mA nominal + load
−15V ±3%	20mA nominal + load
ENVIRONMENTAL & PACKAGING	
Operating Temperature	0°C to 70°C
Storage Temperature	−25°C to +85°C
Relative Humidity	0 to 95%, non-condensing
Modupac™ Dimensions	2" x 2" x 0.375" (50.8 x 50.8 x 9.5mm)
Shielding	RFI 6 sides; EMI 5 sides

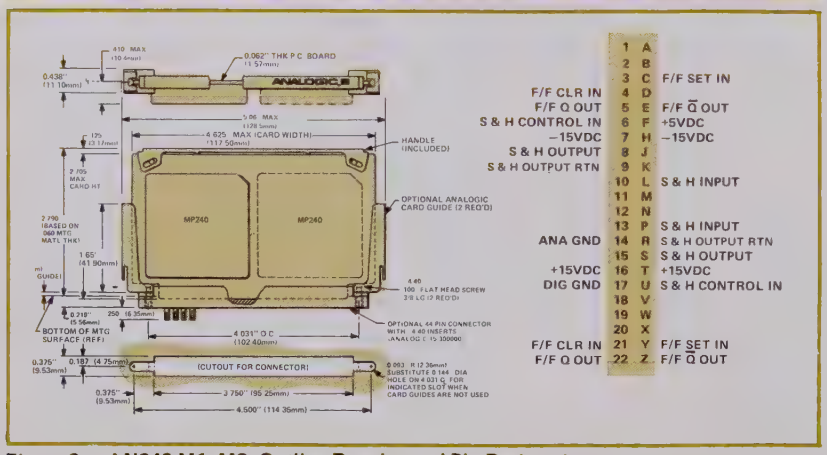
MP240
MP240
HANDLE (INCLUDED)
OPTIONAL ANALOGIC CARD GUIDE (2 REQ'D)
BOTTOM OF MTG SURFACE (REF)
(CUTOUT FOR CONNECTOR)
4.500" (114.35mm)
1 A
2 B
3 C F/F SET IN
F/F CLR IN 4 D
F/F Q OUT 5 E F/F Q̄ OUT
S & H CONTROL IN 6 F +5VDC
−15VDC 7 H −15VDC
S & H OUTPUT 8 J
S & H OUTPUT RTN 9 K
10 L S & H INPUT
11 M
12 N
13 P S & H INPUT
ANA GND 14 R S & H OUTPUT RTN
15 S S & H OUTPUT
+15VDC 16 T +15VDC
DIG GND 17 U S & H CONTROL IN
18 V
19 W
20 X
F/F CLR IN 21 Y F/F SET IN
F/F Q OUT 22 Z F/F Q̄ OUT

Figure 2. AN240 M1, M2 Outline Drawing and Pin Designations

DIELECTRIC ABSORPTION

Dielectric absorption is the decaying of the Hold voltage (on the Hold capacitor) due to the charge redistribution within the capacitor dielectric. This error is a resultant of rapidly charging the Hold capacitor and disconnecting the charge source. The output voltage will decay according to the following relationship:

$$\Delta E = E_s K \log_{10}\left(\frac{t_s + t_h}{t_s}\right)$$

where:

ΔE = Output voltage error
E_s = Capacitor voltage change
K = Empirical constant for Hold capacitor dielectric ($K = 1.5 \times 10^{-4}$ for polystyrene capacitor in MP240)
t_s = Sample time; t_h = Hold time

Example: For a 20V step, a Sample time of 7μs, and a Hold time of 40μs, ΔE <2.5mV.

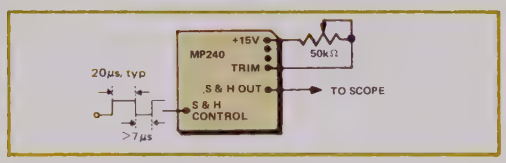

Figure 3. MP240 Offset Adjustment. To adjust for system zero offset, connect external 50-kilohm potentiometer as shown. Apply desired system-zero input, place MP240 in successive Sample & Hold, and adjust for zero output during Hold. If potentiometer is not used, connect trim to +15V with 24kΩ resistor.

ORDERING GUIDE

Simply Specify — 240

For

Modupac™	MP		
PC Card	AN		
Circuit Type		240	
Standard Speed			Blank
Optional Speed			−1
One Module on PC Card (AN only)			M1*
Two Modules on PC Card (AN only)			M2*

* Supplied with external 9948 flip-flop

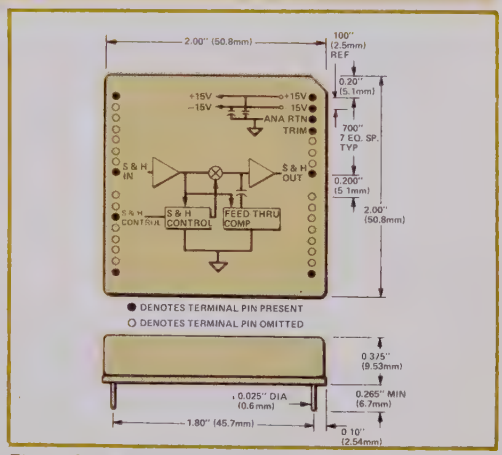

Figure 4. MP240 Outline Drawing

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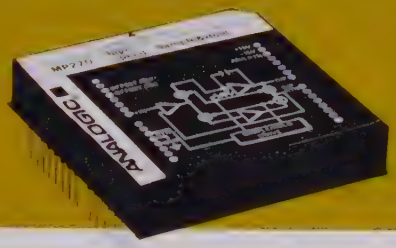

MP270

Very High Speed

SAMPLE & HOLD AMPLIFIER

DESCRIPTION

The Analogic MP270 is the highest speed-with-accuracy sample and hold amplifier available. Its low acquisition time of 1μs, aperture uncertainty time of less than 0.2 ns, and wide bandwidth assure compatibility with data acquisition systems having throughput rates up to 300kHz. The high input impedance of the MP270 combined with its low noise and low feedthrough characteristics assure accuracies of 0.01% at these throughput rates.

PERFORMANCE

The 1 μs maximum acquisition time and the 0.01% accuracy of the MP270 are attained by placing a feedback loop around the switching circuit. This design technique provides compensation for any switching and non-linearity errors within the loop while forcing the output to follow the input. The introduction of very fast switching circuits limits the aperture uncertainty time to within 0.2 ns and virtually guarantees measurement repeatability. The 100-megohm input impedance of the MP270 assures minimal source loading without additional external buffering, and the low hold mode decay rate of 2 microvolts per microsecond assures highly accurate digitization even at slower conversion rates.

Multiplexed digitizing throughput rates at 140kHz with 0.01% accuracy can be achieved by combining the MP270 Sample and Hold Amplifier with the Analogic AN4716 16-channel Multiplexer and the Analogic MP2912A 12-bit Analog-to-Digital Converter. (See Figure 1.) The 140kHz throughput rate is determined by adding the maximum multiplexer settling time (2μs) to the maximum sample & hold acquisition time (1μs) and the 12-bit analog-to-digital conversion time (4μs) — each at 0.01% accuracy — to give a total throughput time of 7μs. The Analogic AN3005 (115V AC input) or MP3020 (+5V DC input) power supply should be used if direct system power is not readily available.

APPLICATION

Because of the exceptionally high accuracy-with-speed performance of the MP270 and its low noise and wide bandwidth characteristics, care must be taken to minimize noise pickup on the signal input leads. All input and control pulse leads should be short and shielded, and a remotely generated control signal should be buffered close to the MP270 to prevent ringing.

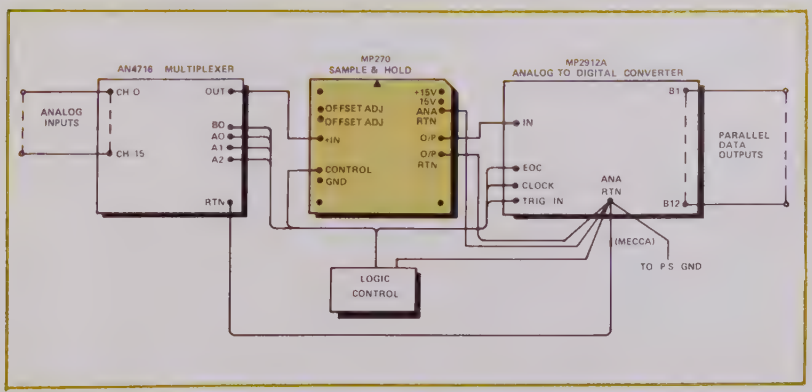

Figure 1. MP270 Sample and Hold Amplifier with MP2912A Analog-to-Digital Converter and AN4716 Multiplexer guarantees a throughput rate of up to 140 kHz for a 12-bit data acquisition application.

FEATURES

- 1μs Maximum Acquisition Time with 0.01% Accuracy
- Wide Bandwidth: 500kHz for Full Power
- High Input Impedance: 10^8 Ohms
- Low Aperture Uncertainty of 0.2ns Guarantees Accurate Digitization
- Low Droop Rate: 2μV/μs

Figure 2. MP270 Output Characteristics Showing Acquisition Time. Upper waveform shows response of MP270 to a 20 volt step input signal. Lower Waveform is a 2500:1 amplification of the upper trace and shows settling characteristics of the MP270.

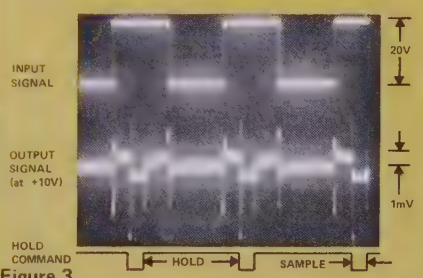

Figure 3. MP270 Output Characteristics showing hold pedestal and feedthrough rejection characteristics. The MP270 samples the input signal only while it is at +10 volts. When the input signal goes to −10 volts, the MP270 hold voltage changes by less than 1mV.

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MP270 SPECIFICATIONS

SAMPLE MODE	
Input Voltage	±10V max. useful signal, ±15V max. without damage
Gain	+1.000 ±0.005%
Small Signal Bandwidth	10 MHz
Full Power Bandwidth	500 kHz min.
Slew Rate	50 V/μs
Input Impedance	10^8 Ω in parallel with 10 pF
Linearity	0.005% max. nonlinearity
Settling Time	
to 0.01% for 20V Step Input	700 ns typ., 900 ns max.
to 0.05% for 10V Input	450 ns typ., 600 ns max.
Input Bias Current	<100 pA
Input Offset Voltage	20mV max., adjustable to zero. See Fig. 5.
Offset Tempco	50μV/°C
Offset vs. Supply	0.0015% FS/% supply voltage change
Noise	300μV p-p max.
SAMPLE TO HOLD SWITCHING	
Switching Transient Settling Time (to 0.01% F.S.)	150 ns typ., 400 ns max.
Aperture Time	10 ns typ.
Aperture Uncertainty Time	±0.2 ns typ.
HOLD MODE	
Output Voltage	±10V max.
Max. Load	500Ω in parallel with 200 pF (short-circuit protected)
Output Impedance	0.1Ω
Droop Rate	2μV/μs
*Dielectric Absorbtion	Approx. 0.0075% @ 2μs Sample time, 5μs Hold time
Voltage Feedthrough (20V p-p 500 kHz Sinusoid on Input)	−80dB
Hold Offset (Pedestal)	±10mV adjustable to zero with externally accessible internal adjustment
Hold Offset Tempco	30μV/°C
Hold Offset Non-Linearity (Pedestal Variation over Input Signal Range)	0.005% max.
Output Voltage variation due to Control Pulse Variation	1mV per volt of change in control signal
Noise	0.5mV p-p max.
HOLD TO SAMPLE SWITCHING	
Acquisition Time	
to 0.01% for 20V Step Input	800 ns typ., 1μs max.
to 0.05% for 10V Step Input	550 ns typ., 700 ns max.
DIGITAL CONTROL INPUT	
Compatibility	TTL compatible, 2 logic loads
Input Impedance	1kΩ in parallel with 33pF (3mA sink current)
Sample	Logic "0" (+0.4V max.)
Hold	Logic "1" (+3.0V min.)
Required Rise Time	10 ns max. to obtain minimum aperture time
POWER SUPPLY	
+15V ±3%	60 mA plus load current
−15V ±3%	40 mA plus load current
ENVIRONMENTAL & PACKAGING	
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−25°C to +85°C
Relative Humidity	0 to 95% non-condensing
Modupac™ Dimensions	2" x 2" x 0.39" (50.8 x 50.8 x 9.9mm)
Electrical Shielding	RFI 6 sides; EMI 5 sides

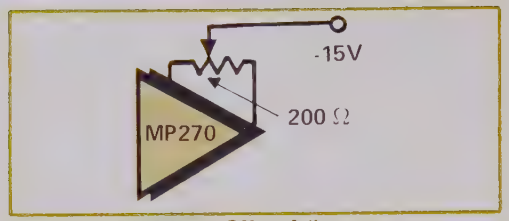

Figure 5. MP270 Input Offset Adjustment

Input voltage offset compensation is accomplished by connecting a potentiometer between the two OFFSET ADJ. terminals. The variable output of the potentiometer is adjusted until the offset is reduced to an acceptable level.

*DIELECTRIC ABSORPTION

Dielectric absorption is the decaying of the Hold voltage (on the Hold capacitor) due to the charge redistribution within the capacitor dielectric. This error is a resultant of rapidly charging the Hold capacitor and disconnecting the charging source. The output voltage will decay according to the following relationship:

$$\Delta E = E_S K \log 10\left(\frac{t_s + t_h}{t_s}\right)$$

where:

ΔE = Output voltage error
E_S = Capacitor voltage change
K = Empirical constant for Hold capacitor dielectric ($K = 1.5 \times 10^{-4}$ for polystyrene capacitor in MP270)
t_s = Sample time; t_h = Hold time

Example: For a 20V step, a Sample time of 2μs, and a Hold time of 5μs, ΔE = 1.5mV.

ORDERING GUIDE

Simply Specify ——— [ ]

For	*Enter*
Modupac™	**MP270**
One MP270 on a PC card	**AN270M1***
Two MP270's on a PC card	**AN270M2***

*Supplied with 9948 RS flip-flop.

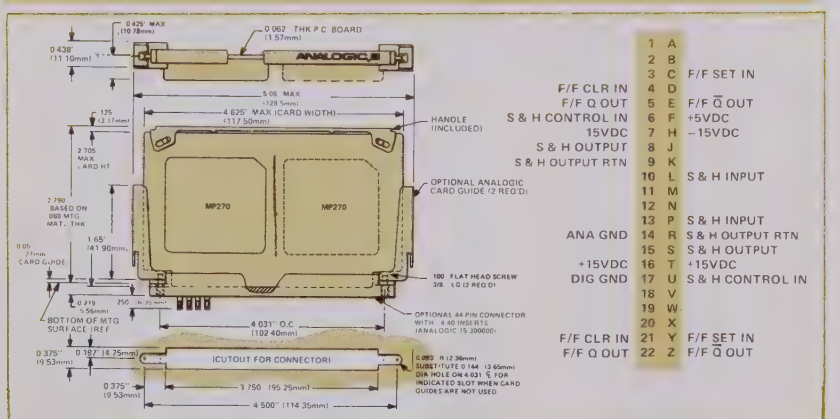

Figure 4. AN270M1, M2 Outline Drawing and Pin Designations.

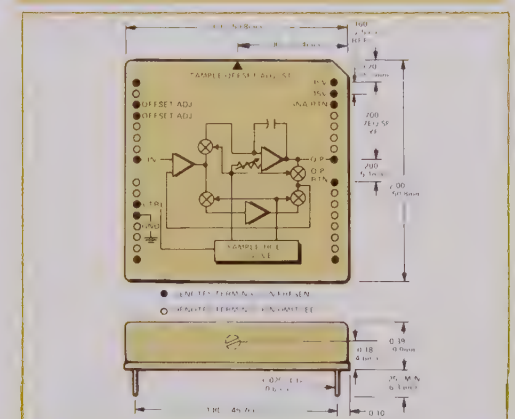

Figure 6. MP270 Outline Drawing

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Bulletin No. 16-100053 REV 4

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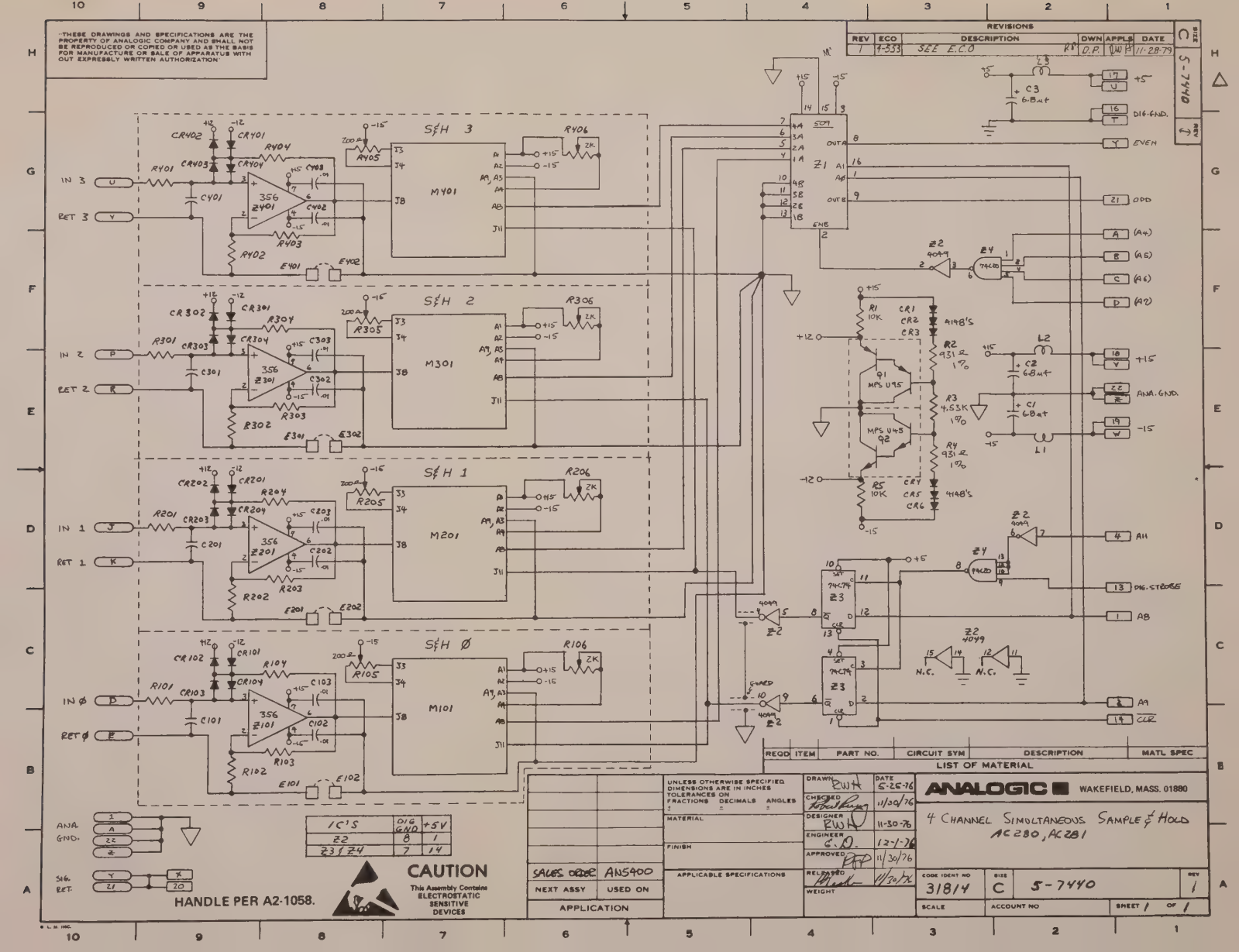
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REVISIONS
REV ECO DESCRIPTION DWN APPR DATE
1 1-333 SEE E.C.O RP D.P. 11-28-79
S/H 3
S/H 2
S/H 1
S/H Ø
M401
M301
M201
M101
IN 3
RET 3
IN 2
RET 2
IN 1
RET 1
IN Ø
RET Ø
ANA. GND.
SIG. RET.
+15
-15
+5
+12
-12
DIG. GND.
EVEN
ODD
AH
AB
AA
CLR
DIG. STROBE
N.C.
1C'S DIG GND +5V
Z2 8 1
Z3 & Z4 7 14
CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.
LIST OF MATERIAL
REQD ITEM PART NO. CIRCUIT SYM DESCRIPTION MATL SPEC
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
SALES ORDER AN5400
NEXT ASSY USED ON
APPLICATION
DRAWN BWH DATE 5-25-76
CHECKED 11/30/76
DESIGNER BWH 11-30-76
ENGINEER 12-1-76
APPROVED 11/30/76
RELEASED 11/30/76
WEIGHT
ANALOGIC WAKEFIELD, MASS. 01880
4 CHANNEL SIMULTANEOUS SAMPLE & HOLD
AC280, AC281
CODE IDENT NO 31814
SIZE C
5-7440
REV 1
SCALE
ACCOUNT NO
SHEET 1 OF 1

AC4050 SERIES

ISOPLEXER FOR AN5400

GENERAL

The Analogic AC4050 Series Isoplexer isolates each of four input signals from common mode voltages up to 300V, with over 160dB of common mode rejection, and multiplexes the isolated differential outputs to the ANDS5400 Bus under system program control. This device is unequalled in terms of common mode voltage isolation, common mode rejection, and its ability to transmit accurately both low and high level signals to the A/D converter.

Fig. 1 illustrates the common mode environments under which the AC4050 transfers its inputs with high accuracy and gain stability. Isolation for each channel is accomplished by a dedicated Analogic MP225A Isolation Amplifier, with adjustable offset, as shown in Fig. 1.

For optimum sensitivity in each group of four channels, the AC4050 Series is available in eleven full-scale ranges, from ± 10mV to ± 10V. Refer to the Ordering Guide for model designations of the respective full scale ranges.

User input connections are made with screw-type connector assembly, Part Number AC86.

SPECIFICATIONS

INPUT

Number of Channels	4 per card.
Common Mode Voltage Per Channel	(See Fig. 2). ± 300V rms, 60Hz (with respect to ANDS5400 ground).
Channel to Channel	± 600V rms 60Hz.
Common Mode Rejection Ratio	> 160dB from dc to 60Hz (4050 to 4054) > 140dB @ 60Hz (4055 to 4060) with 1kΩ source unbalance.
Common Mode Impedance	1000 megohms @ dc.
Pass Band	5Hz with 80dB/decade roll-off.
Normal Mode Rejection Ratio	> 80dB @ 60Hz.
Input Impedance	> 100MΩ @ dc (See Fig. 3).
Input Bias Current	< 10nA.
Input Full Scale Range	(See Ordering Guide).
Maximum Input	115V rms without damage for 5 sec.
Zero Offset	Adjustable to Zero.

ACCURACY

Gain	± 0.01% FSR.
Linearity	± 0.015% FSR.

STABILITY

Offset	± 1μV/°C, RTI (4050-4054). 25μV/°C RTI (4055-4060).
Gain	± 0.0030% FSR/°C.
Noise	1.0μV rms (4050 to 4054). 2.0μV rms (4055 to 4060).

OUTPUT

Type	Differential (Even & Odd Bus of ANDS5400).
Settling Time	5μsec. to ± 0.01% FSR of final value.
Cross-Channel Attenuation	> 80dB.

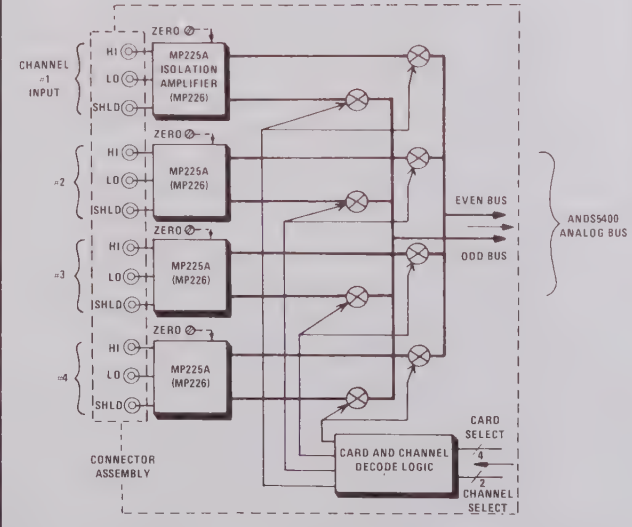
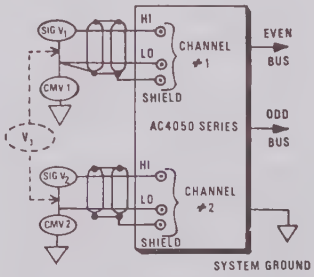


Fig. 1. AC4050 Series, Block Diagram, showing individual OFFSET adjustments



CMV1, CMV2, ≤ 300 VRMS
V3 = CHANNEL TO CHANNEL CMV ≤ 600 VRMS

*Typical connections of SHIELD at Sensor.
Only 2 Of 4 Channels are shown.

Fig. 2. AC4050 Series CMV Specifications and Limitations

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CALIBRATION

Each Input Channel is calibrated at the factory for zero offset. If system applications introduce a change in the offset, or if recalibration is required, proceed as described below. Refer to Fig. 3 for adjustment locations. An extender card may be required to obtain access to the controls.

(1) Place ANDS5400 in local control.
(2) Address channel 00 on the card being calibrated.
(3) Apply the input voltage corresponding to "zero" signal output on the bus.
(4) Adjust offset for channel 0 (R101) for zero indication on ANDS5400.
(5) Address channel 1, repeat Steps (3) and (4), using R201 in Step (4).
(6) Address channel 2, repeat Steps (3) and (4), using R301 in Step (4).
(7) Address channel 3, repeat Steps (3) and (4), using R401 in Step (4).

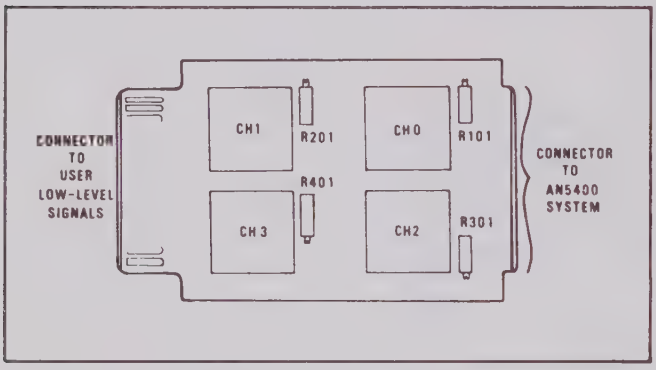

Fig. 3. Location of Offset Adjustments

ADDRESSING

The address structure of the ANDS5400 provides complete flexibility of configuration and installation. Table 1 details the address of devices installed in any enclosure. To determine the absolute address of this device, simply add to the address, listed in Table 1, the enclosure address in the Analog Mode (see ANDS5400 Manual).

Table 1

Address Locations (Octal)

J1	0.	10.	20.	30	J9	400.	410.	420.	430
J2	40.	50.	60.	70	J10	440.	450.	460.	470
J3	100.	110.	120.	130	J11	500.	510.	520.	530
J4	140.	150.	160.	170	J12	540.	550.	560.	570
J5	200.	210.	220.	230	J13	600.	610.	620.	630
J6	240.	250.	260.	270	J14	640.	650.	660.	670
J7	300.	310.	320.	330	J15	700.	710.	720.	730
J8	340.	350.	360.	370	J16	740.	750.	760.	770

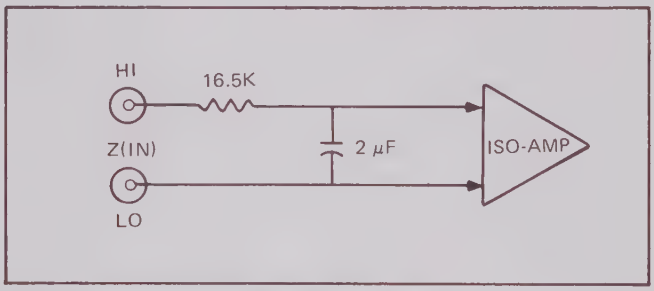

Fig. 4. Input Impedance Equivalent Circuit

CONNECTOR TERMINALS

(Analogic Assembly AC86)

Channel 00 —	Lo	1
	Shield	2
	Hi	3
Channel 10 —	Lo	4
	Shield	5
	Hi	6
	Not Used	7
		8
		9
Channel 20 —	Lo	10
	Shield	11
	Hi	12
Channel 30 —	Lo	13
	Shield	14
	Hi	15

ORDERING GUIDE

To Order Full Scale Range		Specify
± 10mV	Use MP225A Amplifier	AC4050
± 20mV		AC4051
± 40mV		AC4052
± 80mV		AC4053
± 160mV		AC4054
± 320mV	Use MP226 Amplifier	AC4055
± 640mV		AC4056
± 1.25V		AC4057
± 2.5V		AC4058
± 5.0V		AC4059
± 10.0V		AC4060

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AC4250 SERIES

THERMOPLEXER FOR AN5400

GENERAL

The Analogic AC4250 Series THERMOPLEXER isolates each of four themocouple input signals from common mode voltages up to 300VRMS with over 160dB of common mode rejection, and **multiplexes** the **cold-junction-compensated** and **isolated** outputs to the AN5400 Bus under system program control. Figure 1 illustrates the harsh common mode environments under which the AN5400 transfers the inputs with accurate and stable gain.

Figure 2 illustrates the manner in which the "cold junction" sensing element in the connector assembly develops a signal which is calibrated for the specified thermocouple and by which the compensation is inserted as an offset in the ODD bus line.

Isolation for each channel is obtained by using the Analogic MP225 Isolation Amplifier, and this provides an independent open-thermocouple detection and an offset adjustment for each channel in the card. The open-thermocouple detection circuit pulls up the HI line to an over-range voltage, as illustrated in Figure 3.

The AC4250 Series may be ordered for any one of seven commonly used standard thermocouple types: B, E, J, K, R, S, and T, to provide users with the capability of monitoring temperatures from −270°C to +1800°C. Refer to the Ordering Guide to select the particular Thermoplexer for the thermocouple to be used.

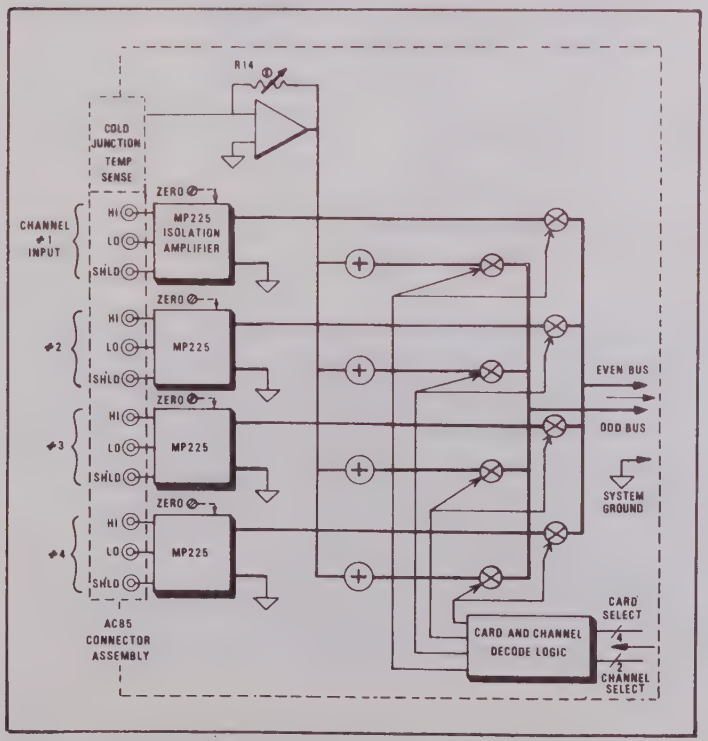

Fig. 2. AC4250 Series Block Diagram, showing individual OFFSET adjustments and Cold Compensation

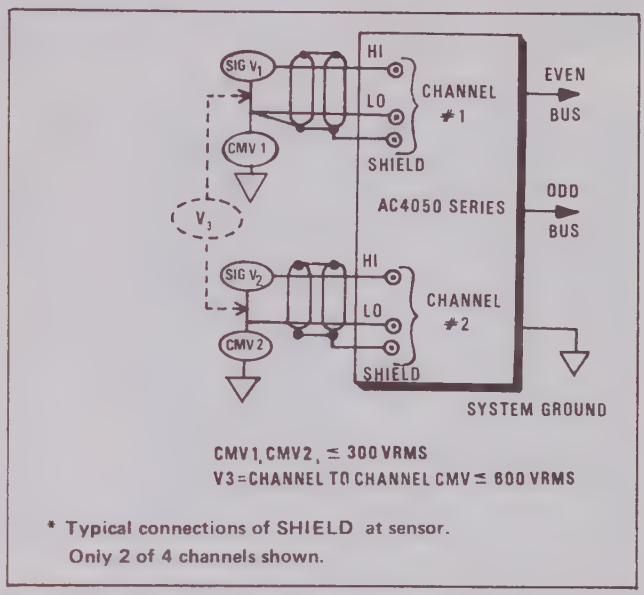

Fig. 1. AC4250 Series CMV Specifications & Limits

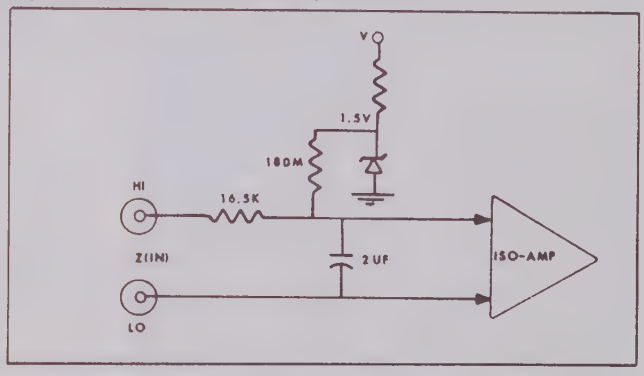

Fig. 3. Input Impedance Equivalent Circuit Schematic

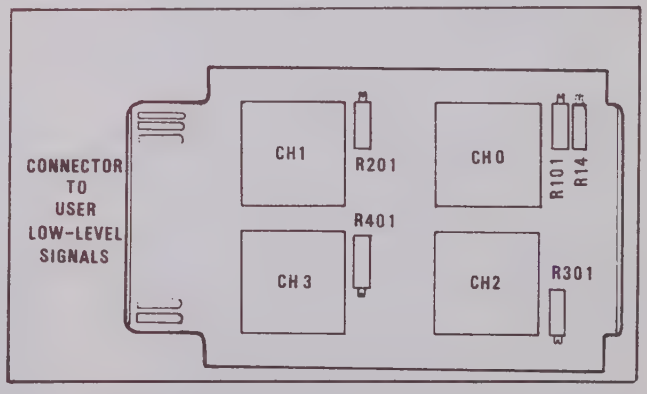

Fig. 4. Location of OFFSET & Cold Junction Comp. Adjust.

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CALIBRATION

A uniform cold-junction compensation is applied to all four channels of an AC4250 Series card, and it is factory-calibrated for the designated themocouple, while the zero offset is factory calibrated for a zero offset in each channel. The following procedures, performed in the sequence shown, may be used to recalibrate the cold-junction compensation or to correct for individual channel non-zero effects. Refer to Figure 4 to locate adjustment controls. An extender card may be required to obtain easy access to them.

A. Channel Zero Offset

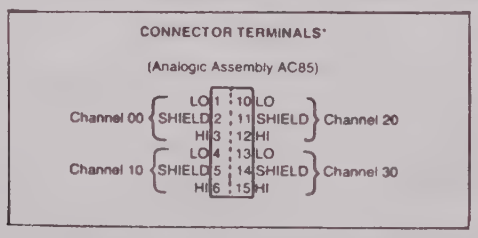
(1) Place AN5400 in local control.
(2) Remove the normal thermocouple input connections for Channel 00.
(3) Short the input terminals for Channel 00. (See Table of Terminal Connections.)
(4) Program the AN5400 to indicate the EVEN bus output (with respect to system ground) for the card and channel being adjusted.
(5) Adjust R101 for zero indicated output.
(6) Remove the shorting link; replace the thermocouple connections.
(7) Repeat steps (2) through (6) above for channels 10, 20, and 30, using R201, R301, and R401, respectively in step (5).

B. Cold-Junction Compensation

(8) Place AN5400 in local control.
(9) Program the AC4250 Series card and select the differential output for one of the channels that has been zero-calibrated as in steps (1) through (7) of procedure A above.
(10) Insert the thermocouple for the channel selected in step (9) above into an ice bath of 0°C, or use a reference ice point thermocouple source in place of the system thermocouple.
(11) Adjust R14 for zero indicated output of that channel.

C. Channel Non-Zero Offset

For any channel in which system-induced non-zero effects are to be adjusted, proceed as follows after performing steps (1) through (11) in A and B above.
(12) Place AN5400 in local control.
(13) Select the AC4250 Series card and that channel for which the installed thermocouple is to be offset-adjusted. Program the AN5400 to indicate the differential output of that channel.
(14) Insert the channel thermocouple into a measured environment where the temperature is accurately known (Ice Bath, for example).
(15) Adjust the corresponding offset control for that channel's isolation amplifier for the desired AN5400 output indication.



SPECIFICATIONS

Input

Thermocouple Types:	7 (B, E, J, K, R, S, T)
Number of channels:	4 per card
Common Mode Voltage:	(see Figure 1)
Per Channel:	±300V RMS, 60Hz (wrt AN5400 ground)
Channel to Channel:	±600V RMS 60Hz
Common Mode Rejection Ratio:	>160dB from DC to 60Hz with 1 KΩ source unbalance
Common Mode Impedance:	1000 megohms
Pass Band:	5Hz with 80dB/decade roll off
Normal Mode Rejection Ratio:	>80dB @ 60Hz
Input Impedance:	>100MΩ @ DC (see Figure 3)
Input Bias Current:	<10nA **Open Ckt. Detect.**
Input Full Scale Range:	(see ordering guide)
Maximum Input:	115VRMS without damage
Zero Offset:	Adjustable to Zero

Accuracy

Gain:	±0.01% FSR
Linearity:	±0.015% FSR
Cold Junction Comp:	±1°C over ambient temperature of ±10°C at connector

Stability

Offset:	±1μV/°C, referred to input
Gain:	±0.0025% FSR/°C
Noise:	1.0μVRMS
Tempco of Cold Junction Comp:	±0.01°C/°C

Output

Type:	Differential (Even & Odd Bus of AN5400)
Settling Time:	5μ seconds to ±0.01% FSR of final value
Cross Channel Attenuation:	>80dB

ORDERING GUIDE

To Use AC4250 Series Themoplexer with Thermocouple Type	Specify
B	AC4256
E	AC4253
J	AC4252
K	AC4251
R	AC4254
S	AC4255
T	AC4250

*** Terminal 7 = System Ground.**
Terminals 8 and 9 not available to user.

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AVAILABLE FROM:

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MP225A LOW NOISE, LOW LEVEL ISOLATION AMPLIFIER AND MP235 DRIVER

DESCRIPTION

The Analogic MP225A is a unique Isolation Amplifier which accepts low-level signals in the presence of very high level common mode voltages and amplifies them, producing clean and accurate output signals. As indicated in Fig. 1, the MP225A consists of three basic sections: a stabilized input chopper amplifier, an isolating coupler and an output amplifier/filter section. The unusual design of the MP225A provides 160dB of common mode rejection, and ensures unsurpassed performance in the presence of common mode voltages as high as 1000V peak.

The MP225A Isolation Amplifier offers user-selectable gains from 100 to 1000; input voltage ranges up to ±100mV full scale; less than 1μV RMS input noise from DC to 5Hz; linearity better than 0.015% FSR and an input impedance of 100MΩ minimum at DC. Featuring a CMRR of 160dB and a common mode impedance in excess of 1000MΩ at DC, this remarkable unit exhibits exceptional stability with an offset voltage tempco of only 0.5μV/°C.

The MP225A requires an external square-wave power drive of approximately 27V peak at 20kHz. A compatible Power Driver module, the MP235, is available for driving up to eight Isolation Amplifiers. Both the MP225A and MP235 are packaged in compact, fully shielded metal cases.

APPLICATION

The MP225A Isolation Amplifier offers value-added performance for monitoring a wide range of thermocouple, strain gage and other low-level DC signals. Its superior input/output isolation, relative immunity to high common mode voltages and low noise performance make it particularly appropriate for accurate and precise measurement of low signal levels in harsh industrial environments.

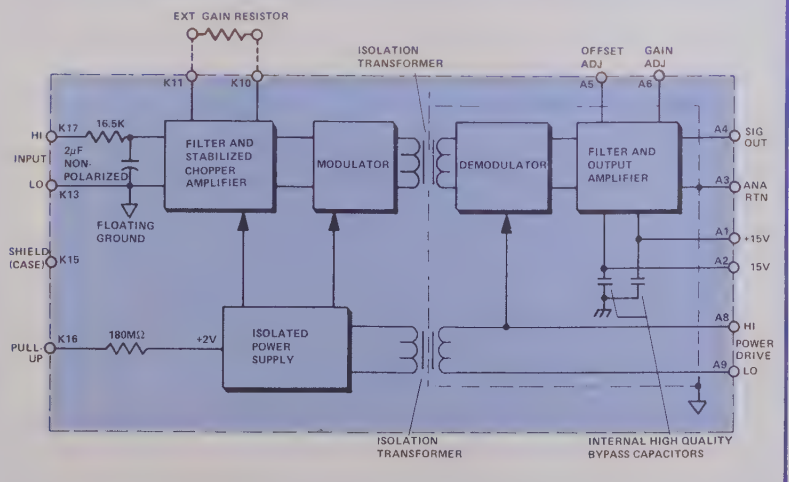

Fig. 1. MP225A Isolation Amplifier Functional Block Diagram.

FEATURES

- Superior Isolation between Input and Output
  CMRR: 160dB
  CMV: 1000V Peak.
- Optimized for Thermocouples and Strain Gages
  ±10mV to ±100mV Full Scale Input Ranges.
- Chopper-Stabilized Input Amplifier
  ±0.5μV/°C Offset Tempco.
- Low Noise Operation
  < 1μV RMS, DC to 5Hz.
- High Linearity
  0.015% FSR Max.
- 4-Pole Roll-Off From 5Hz.
- High Common Mode Impedance
  > 1000 MΩ at DC.
- Low Output Impedance
  < 0.1 Ω.
- Low Gain Tempco
  ±20ppm FSR/°C.
- Open Input Circuit Indicator.
- Output Short-Circuit Protected to Ground.

APPLICATIONS

- Thermocouple Temperature Measurements.
- Weighing Systems.
- Strain Gage Measurements.
- Remote Data Acquisition and Precision Telemetry Systems.
- Geophysical Instrumentation.
- Microvolt and Millivolt-Level Measurements.

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MP225A SPECIFICATIONS

ANALOG INPUT

Input Voltage Range	±10mV to ±100mV, full scale.
Gain Range	100 to 1000, non-inverting, resistor-programmable.
Gain Accuracy	Factory trimmed to within ±0.1% gain uniformity.
Input Amplifier Type	Isolated, chopper.
Bias Current	1nA max.; 10nA max. with open-thermocouple indicator connected.
Common Mode Isolation Voltage	1000V DC, 750V RMS (test).
Common Mode Rejection Ratio	160dB @ 60Hz with 1kΩ source unbalance. See test circuit in Fig. 4.
Common Mode Impedance	> 1000 MΩ @ DC; > 10 MΩ @ 60Hz.
Differential Input Impedance	100 MΩ DC resistance shunted by RC network. (See Note 1).
Noise (DC - 5Hz)	1μV RMS, Max., RTI.
Maximum differential Input	120V RMS @ 60Hz , 5 secs., without damage.
Offset Voltage	Adjustable to zero. (See Note 2).
Offset Adjustment Range	±50mV, referred to output.
Bandwidth	DC - 5Hz.
Filter Type	2-pole input, 2-pole output; 80dB/decade over-all.
Open Input Indicator	Pin-selectable. Open circuit between HI and LO, indicated by positive saturation at output.

ANALOG OUTPUT

Voltage Range	±10V, full scale.
Output Impedance @ DC	< 0.1Ω
Maximum Load	5mA, 500 pF shunt capacity.
Output Circuit Protection	Output short-circuit protected to ground.
Linearity	±0.015% FSR max.

STABILITY

Tempco of Offset Voltage	0.5μV/°C typ., 1μV/°C Max., for gain = 1000.
Power Supply Rejection Ratio	> 54dB.
Warmup Time	5 minutes to specified accuracy.
Gain Tempco	±20ppm FSR/°C typ., ±30ppm FSR/°C max.

DC POWER REQUIREMENTS

Supply Voltage	+15V, −15V, ±3%.
Supply Current	3.3mA, Max.

AC POWER REQUIREMENTS (SEE NOTE 3)

Coupler and Chopper Drive	Two square-wave drive signals of complementary phase. (Pins A8 & A9).
V_{IH}	Between +13V and V+.
V_{IL}	Between −13V and V−.
Drive Current	3mA typ., 5mA Max.
Risetime (10% - 90%)	200ns Max.
Skew Time Between 50% points	50ns Max.

MP235 SPECIFICATIONS

Output Drive	Compatible with above MP225A requirements.
Maximum Loading	Eight MP225A.
Frequency	20.8 kHz ±1%.
Supply Voltage	+15V, −15V, ±3%.
Supply Current	5mA x (1 + Number of MP225A's) Max.

ENVIRONMENTAL AND PACKAGING (BOTH UNITS)

Operating Temperature Range	0 to 70°C.
Storage Temperature	−25°C to +85°C.
MP225A Dimensions	2 x 2.4 x 0.5 in. (50 x 60 x 13mm).
MP235 Dimensions	1 x 2 x 0.4 in. (25 x 50 x 10mm).
Shielding	RFI: 6 sides.

Note 1: Input circuit consists of RC filter with R = 16.5kΩ and C = 2μF. See Fig. 1.

Note 2: If an offset trimpot is not used, the output demodulator/amplifier will have an output offset of 10mV, maximum, independent of gain.

Note 3: These specifications are met by the companion driver module, MP235.

OPERATION DATA

SETTING THE MP225A GAIN

The gain of the MP225A may be set to any value from 100 to 1000 by connecting an external resistor of the appropriate value as shows in Fig. 2. Refer to Table 1 for the required resistor values. The MP225A is factory-calibrated to within 0.1% of the GAIN resistor tolerance with the Trim Resistor set to 100 ohms.

The gain of the MP225A may be set to any value from 100 to 1000 by connecting two resistors, as shown in Fig. 2. The GAIN RESISTOR sets the input amplifier gain, and should have a low temperature coefficient (RN55C or better). See Table 1 for the proper resistance value. The TRIM RESISTOR completes the output amplifier feedback circuit and is in series with an internal 20K precision resistor. The MP225A is factory-calibrated to within 0.1% gain accuracy with a trim resistance of 100 ohms.

If adjustable gain trimming is desired, substitute a potentiometer of approximately 200 ohms for the TRIM RESISTOR. Power is negligible and the temperature coefficient is not critical. Trim sensitivity is 0.005% per ohm. With a 200-ohm trimpot, total adjustment range is ±0.5%.

OFFSET ADJUSTMENT

Provision is made for an external offset adjustment on the MP225A Isolation Amplifier. Connect a 50 k ohm (100 ppm/°C or better) multi-turn potentiometer as shown in Fig. 2. To adjust, momentarily short the HI, LO and Shield input connections of the amplifier to the output analog return and set the OFFSET potentiometer for zero output at the SIG OUT terminal.

If an offset pot is not used, the MP225A will exhibit a DC offset not exceeding 10 millivolts output, essentially independent of the gain.

OPEN INPUT INDICATOR

The Pull-Up terminal provides a source current of approximately 10 nA. If open input indication is desired, connect this terminal to the HI Input terminal. In the absence of a complete signal return path at the input, the injection of this current will saturate the amplifier output at its full positive value. Because of the presence of a filter capacitor in the input circuit this action will require approximately one minute for full saturation of the output circuit.

SHIELD CONNECTION

The metal case of the MP225A is electrically insulated from the circuit components and is brought out to terminal K15. For best common mode rejection, the case should be tied either to the low input terminal or, if the input cable is a shielded pair, to the shield as shown in Fig. 2.

OSCILLATOR SYNCHRONIZATION

A single MP235 can drive up to eight MP225A amplifier modules. If more channels are required in the same card rack, the additional MP235 drivers should be synchronized by feeding the OSC OUT signal from one "master" MP235 to the DRIVE INPUT terminals of all MP235's. The remaining OSC OUT terminals should be disconnected. Disable the slave oscillators by connecting the OSC RESET terminal to +15V. The master oscillator RESET should be grounded. The Drive Input is 15V CMOS-compatible.

Thermocouple Type	NBS 125* Temp. Range (°C)	Input Voltage Range (mV)	Over-all Gain	Value of GAIN Resistor (Ohms)**	
B	0 to +1820	±14	714.29	71,229	(71.5K)
E	-270 to +1000	±77	129.87	12,787	(12.7K)
J	-210 to +1200	±43	232.56	23,056	(23.2K)
K	-270 to +1372	±55	181.82	17,982	(17.8K)
R	-50 to +1768	±22	454.55	45,255	(45.3K)
S	-50 to +1768	±19	526.32	52,432	(52.3K)
T	-270 to +400	±21	476.19	47,419	(47.5K)
For other gains between 100 and 1000 use the following formula: GAIN RESISTOR (Ohms) = $200\left[\frac{\text{Gain}}{2}-1\right]$		±10	1000	99,800	(100K)
		±20	500	49,800	(49.9K)
		±50	200	19,800	(20.0K)
		±100	100	9,800	(9.76K)

* NBS Monograph 125, "Thermocouple Reference Tables Based on the IPTS-68", March 1974.

** An RN55C (or better) resistor is recommended. The first values shown are exact. The MP225A is factory-trimmed to within ±0.1% gain error, based on these resistances. The values in parentheses are standard 1% MIL BELL values, and are within the range of the trim potentiometer for zero-error trimming.

Table 1. MP225A Suggested GAIN Resistor Values for Various Thermocouple Temperature and Input Voltage Ranges.

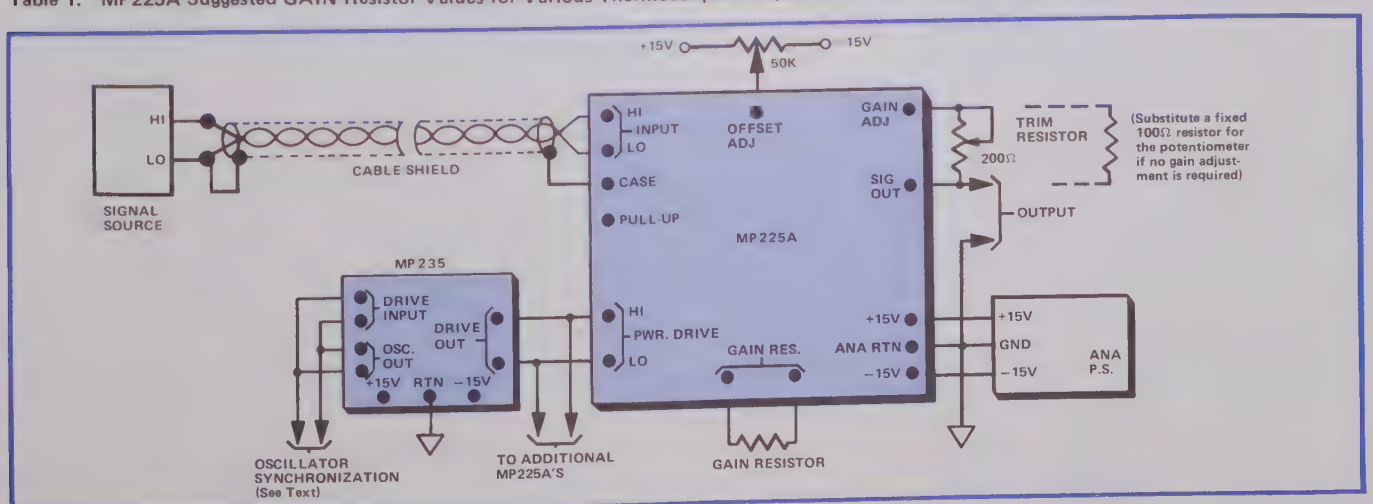

Fig. 2. MP225A and MP235 Connection Diagram.

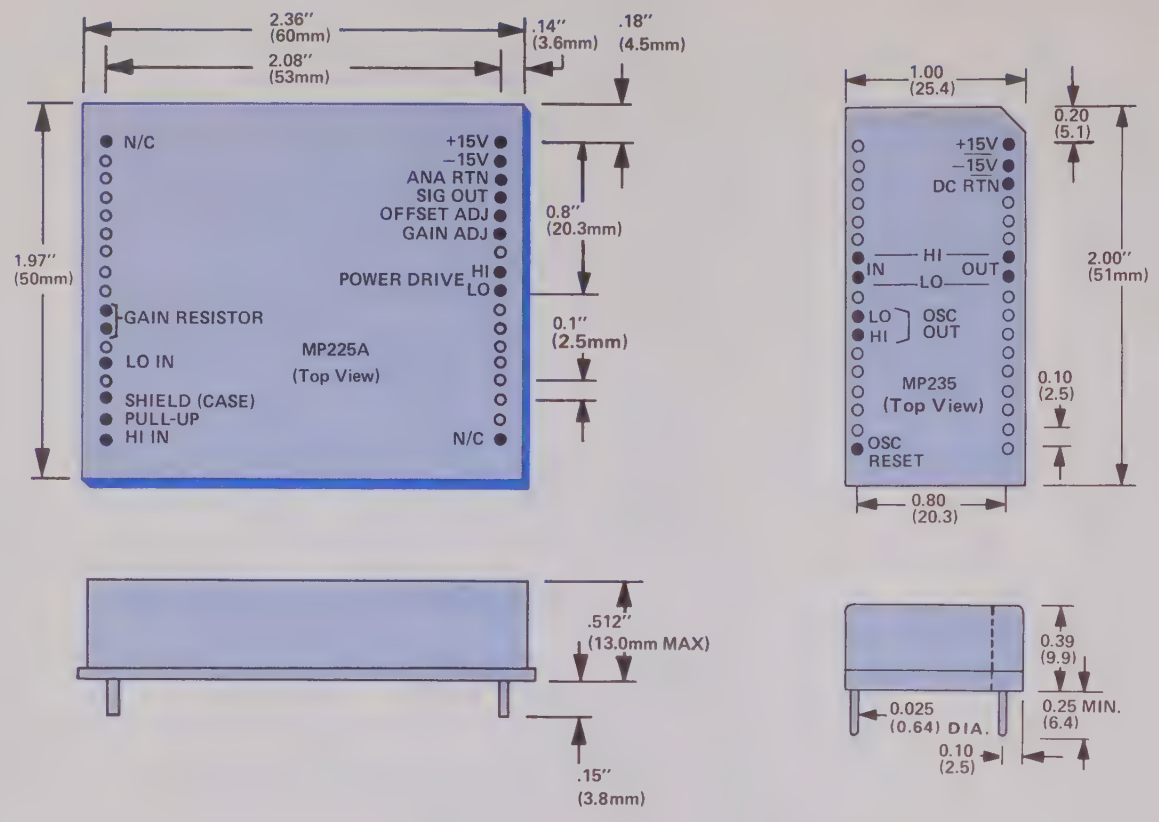

Fig. 3. MP225A and MP235 Outline Drawings, Mounting Dimensions and Terminal Identifications.

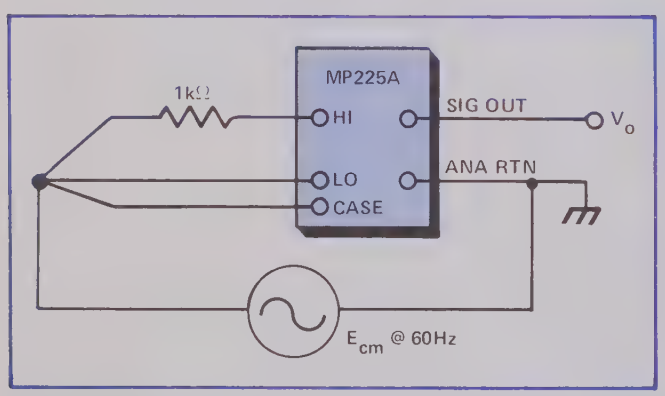

Fig. 4. CMRR Test Circuit.

ORDERING GUIDE

Simply specify: MP225A for Isolation Amplifier

MP235 for companion Power Driver.

At least one MP235 required for every eight MP225A's.

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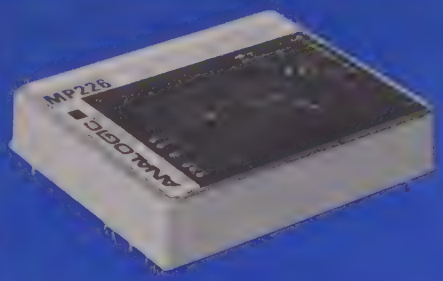

ANALOGIC

MP226 LOW NOISE, HIGH LEVEL ISOLATION AMPLIFIER AND MP235 DRIVER

DESCRIPTION

The Analogic MP226 is an instrumentation-grade Isolation Amplifier designed as a high level companion to the MP225A thermocouple-level unit. It accepts signals in the range of ±100 millivolts to ±10 volts full scale, and has excellent common mode rejection (140dB) and isolation (1000 volts). Because of the careful control of all error sources, the MP226 will support accurate A/D conversion of 12 bits or better.

As shown in Fig. 1, the MP226 consists of three basic sections: A high impedance input amplifier with low pass filter, an isolating coupler, and a low impedance output amplifier and filter

A novel flux-canceling coupler design provides better than 0.015% linearity over the full 20-volt output swing, while maintaining five decades of dynamic range. Other features include a 4-pole (24dB/octave) roll-off from 5Hz, and output short-circuit protection to ground.

The MP226 Isolation Amplifier offers resistor-programmable gains from 1 to 100 and an output voltage range of ±10 volts. The differential input impedance is 100MΩ minimum at dc and common mode impedance is in excess of 1000MΩ at dc. The unit exhibits excellent stability with a gain tempco of only 20ppm FSR/°C.

The MP226 requires an external square-wave power drive of approximately 27V p-p at 20kHz. A compatible Power Drive module, the MP235, is available for driving up to six Isolation Amplifiers. Both the MP226 and MP235 are packaged in compact, fully-shielded metal cases.

The superior input/output isolation offered by the MP226, together with its relative immunity to high common mode voltages, make it particularly appropriate for accurate and precise measurements in harsh industrial environments.

FEATURES

- Superior Isolation
  CMRR: 140dB @ 60Hz
  CMV: 1000V Peak
- Optimized for High Level Signals
  ±100mV to ±10V Full Scale Input Ranges
- High Linearity
  0.015% FSR max.
- Low Noise Operation
  2μV rms max. (RTI)
- High Input Impedance
  100MΩ min. at dc
- High Common Mode Impedance
  >1000MΩ at dc
- Low Output Impedance
  <0.1Ω at dc
- Low Gain Tempco
  ±20ppm FSR/°C
- Open Input Circuit Indicator
- Output Short-Circuit Protected to Ground

APPLICATIONS

- Data Acquisition Systems
- Control Systems
- High Voltage Sensing via Dividers
- 4-20mA Current-to-Voltage Conversion

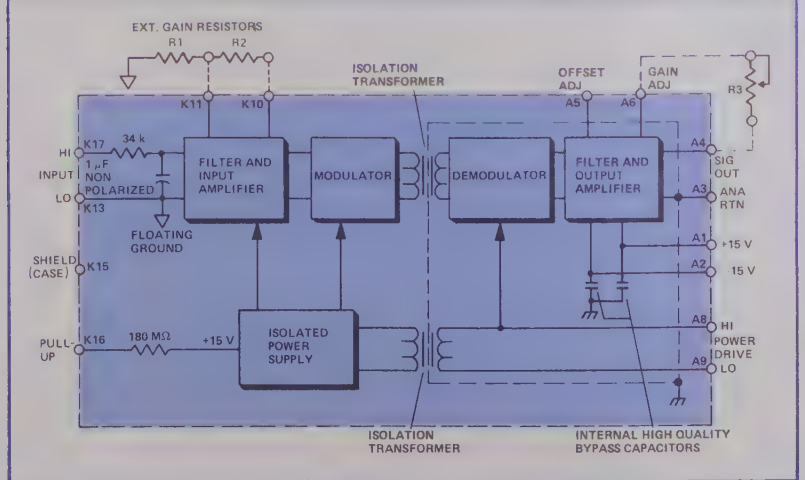

Fig. 1. MP226 Isolation Amplifier Functional Block Diagram.

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MP226 SPECIFICATIONS

ANALOG INPUT

Input Voltage Range	±100mV to ±10V, full scale.
Bias Current	10nA max.
Differential Input Impedance	100MΩ shunted by RC series network (See Note 1).
Noise (dc-5Hz)	2μV rms max., RTI.
Isolation Voltage	1000Vdc, 750V rms (Test).
Common Mode Rejection Ratio (@ Gain = 100)	140dB @ 60Hz with 1kΩ unbalance (see Fig. 5).
Common Mode Impedance (@ Gain = 100)	>1000MΩ @ dc; >10MΩ @ 60Hz.
Maximum Differential Input without damage	120V rms @ 60Hz, for 5 secs.
Offset Voltage	Adjustable to Zero.
Offset Adjustment Range	±50mV, referred to output.
Bandwidth	dc to 5Hz.
No. of Poles	4.

ANALOG OUTPUT

Voltage Range	±10V FSR.
Output Impedance @ dc	<0.1Ω.
Maximum Load Current	±5mA.
Maximum Load Capacitance	500pF.
Output Circuit Protection	Output short-circuit protected to ground.
Linearity	±0.015% FSR max.
Gain Range	1 to 100, externally set via gain resistors. Also adjustable via external potentiometer.
Broadband Output Noise	20μV typ., 30μV max., peak-to-peak, in 1kHz Bandwidth. See Output Noise in text.

STABILITY

Tempco of Offset Voltage	25μV/°C max. RTI. 100μV/°C max. RTO.
Power Supply Rejection Ratio	0.002% FSR/% change in power supply, max., for Offset pot. not connected. 0.005% FSR/% change in power supply, typ., for Offset pot. at end of range.
Warmup Time	5 min. to specified accuracy.
Gain Tempco	20ppm/°C typ., 30ppm/°C max., including external gain resistors with TC match of 10ppm/°C.

DC POWER REQUIREMENTS

Isolation Amp ±15Vdc (V+),(V−) ±3%	2.2mA typ., 3.3mA max. (pins A1 & A2).

AC POWER REQUIREMENTS

(See Note 2)

Coupler and Chopper Drive	Two square-wave drive signals of complementary phase. (Pins A8 & A9).
V_{IH}	Betwen +13V and V+.
V_{IL}	Between −13V and V−.
Drive Current	5mA typ., 8mA max.
Risetime (10%-90%)	200ns max.
Skew Time Between 50% points	50ns max.

MP235 SPECIFICATIONS

Output Drive	Compatible with above MP226 requirements.
Maximum Loading	Six MP226's.
Frequency	20.8kHz ±3%.
Supply Voltage	+15V, −15V ±3%.
Supply Current	8mA x (1 + Number of MP226's) max.
Osc. Out Drive	±2mA typ., ±0.6mA min.
Osc. Input Loading	
Leakage Current (HI or LO)	2μA typ.
Input Capacitance	10pF typ.

ENVIRONMENTAL AND PACKAGING

Operating Temperature Range	0 to 70°C.
Storage Temperature	−25°C to +85°C.
Relative Humidity	0-85%, non-condensing up to +40°C.
Mechanical Dimensions	50 x 60 x 13mm (2 x 2.3 x 0.5 in.).
RFI Shielding	6 sides.

Note 1: Input circuit consists of RC filter with R = 34kΩ and C = 1μF as shown in Fig. 1.
Note 2: These specifications are met by the companion module, MP235.

SETTING THE MP226 GAIN

The voltage gain, A, may be set to any value from 1 to 100. For A >1, three resistors are needed: resistors R1 and R2 determine the center value of A, while R3 acts as a vernier for precision gain trimming. When R3 is set to its nominal value (100 ohms) the value of A is given to an accuracy of 0.1% by the relation,

$$A = 1 + \frac{R2}{R1}$$

The gain temperature coefficient of the MP226 depends primarily on the tempco's of R1 and R2; type RN55C resistors, or better, are recommended. For best stability, the parallel combination should lie between 25 and 40kΩ.

PRECISION TRIMMING

The MP226 gain may be fine-trimmed by varying the value of R3 above or below 100Ω. The change in A is given by,

$$\Delta A = \frac{\Delta R3}{200} \text{ percent per ohm}$$

R3 may be either a fixed trim resistor (1/8W or larger) in the range of 0 to 200Ω, or a trimpot of approximately 200Ω. Since the effect of R3 is divided by a factor of 200, the resistor type is less critical; however, an RN55C resistor or Cermet trimpot is recommended for best long-term stability. If R3 is replaced by a shorting link, the MP226 gain will be reduced by 0.5%, but the stability will be unaffected.

UNITY GAIN

For A = 1, omit R1, and use a resistor of approximately 33kΩ for R2. In this follower application, R2 is non-critical. The MP226 is factory-trimmed for A = 1 ±.001, from 0 to 0.1Hz, with R3 set to 100Ω.

OUTPUT NOISE

Because it is difficult to avoid capacitance between the Power Drive input and the output connections of the MP226, one must take care that output noise spikes do not introduce errors in the following instrumentation. It is recommended that the MP226 be followed either by an integrating-type A/D converter or, if the following device is of wide bandwidth, that a simple RC filter be placed at the device input.

When operated into an integrating A/D converter, the MP226 will typically exhibit a noise level of 2μV rms, referred to its input. When operated into a wideband device, the noise from the output section will dominate, causing the equivalent input noise to be a function of gain. Broadband output noise is roughly proportional to roll-off frequency of the following circuit, and runs about 20μV peak-to-peak in a 1kHz band.

SHIELD CONNECTION

The metal case of the MP226 is electrically insulated from the circuit components and is brought out to terminal K15. For best common mode rejection, the case should be tied either to the low input terminal or, if the input cable is a shielded pair, to the shield as shown in Fig. 2.

OFFSET ADJUSTMENT

Provision is made for an external offset adjustment on the MP226 Isolation Amplifier. Connect a 50k-ohm (100ppm/°C or better) multi-turn potentiometer as shown in Fig. 2. To adjust, momentarily short the HI, LO and Shield input connections of the amplifier to the output analog return and set the OFFSET potentiometer for zero output at the SIG OUT terminal.

If an offset pot. is not used, the MP226 will exhibit a dc offset not exceeding 10 millivolts output, essentially independent of the gain.

OPEN INPUT INDICATOR

The Pull-Up terminal provides a source current of approximately 100nA. If open input indication is desired, connect this terminal to the HI input terminal. In the absence of a complete signal return path at the input, the internal floating (+15V) pull-up voltage will saturate the amplifier output at its full positive value. Because of the presence of a filter capacitor in the input circuit, this action will involve a period of time dependent on the selected input voltage scale. The time, T, required to saturate the amplifier, may be determined with the aid of the following expression:

$$T = 180\,\ell n\left[1 - \frac{V_{FS} - V_{in}}{15\text{ V} - V_{in}}\right] \text{ seconds}$$

where, V_{FS} = selected full-scale input voltage
V_{in} = voltage on 1μF capacitor at instant when indication occurs (see Fig. 3).

Fig. 3 shows the input circuit elements involved in the Open Input Indicator.

OSCILLATOR SYNCHRONIZATION

A single MP235 can drive up to six MP226 amplifier modules. If more channels are reguired in the same card rack, the additional MP235 drivers may be synchronized by feeding the OSC OUT signal from one "master" MP235 to the DRIVE INPUT terminals of all MP235's. The remaining OSC OUT terminals should be disconnected. Disable the slave oscillators by connecting the OSC RESET terminal to ±15V. The master oscillator RESETs should be grounded. The Drive Input is 15V CMOS-compatible. An MP235 oscillator is capable of driving up to 30 slave oscillators.

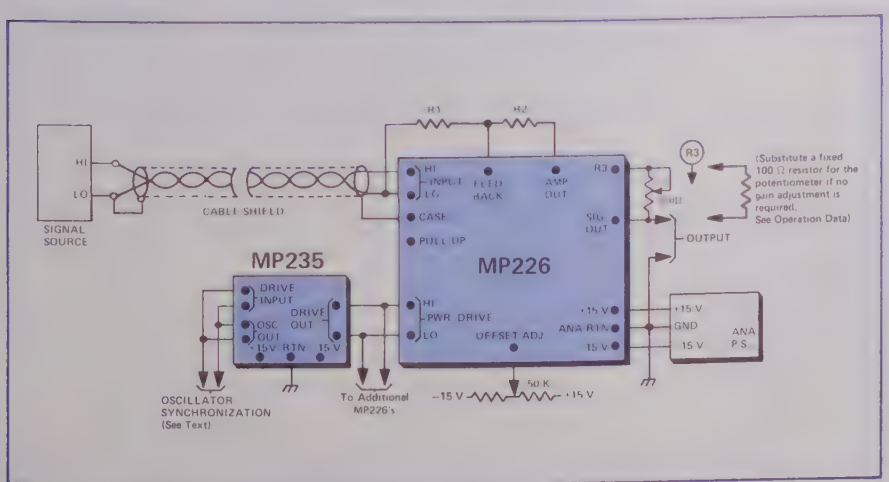

Fig. 2. MP226 and MP235 Connection Diagram.

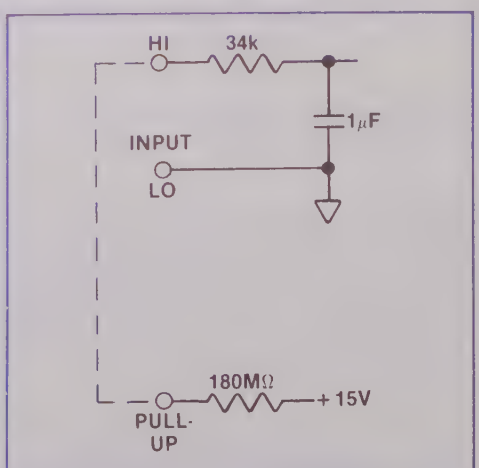

Fig. 3. Open Input Indicator Circuit.

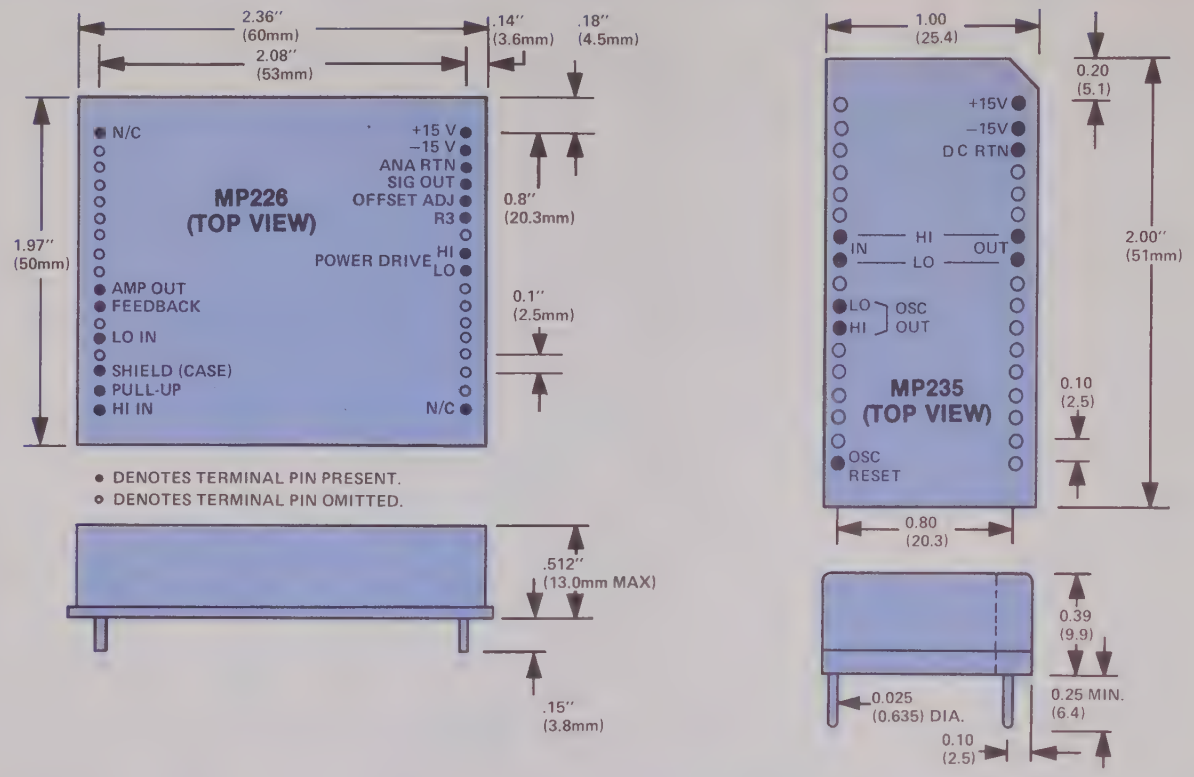

Fig. 4. MP226 Outline Drawings, Mounting Dimensions, and Terminal Identifications.

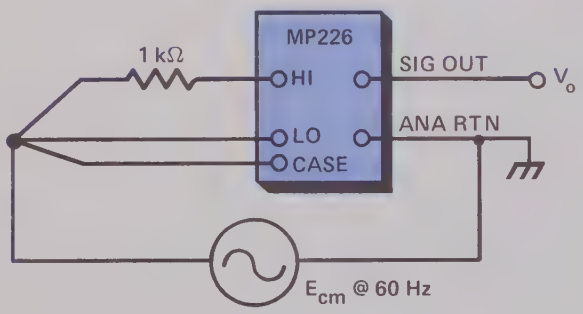

Fig. 5. CMRR Test Circuit.

ORDERING GUIDE

Simply specify: MP226 for Isolation Amplifier.

MP235 for Companion Power Driver.

At least one MP235 required for every six MP226's

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REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPVD	DATE
A	4-3086	SEE ECO	JAR	RJB	5 31 77
B	4-3133	SEE ECO	JAR	JJL	6-8-77
C	4-3145	DRAWING NO. WAS 5-8632 REV B	JAR	JJL	6-28-77
D	4-3207	SEE E.C.O.	DR	JJL	8-24-78

5-8632 D

CH00 M101 — CH10 M201 — CH20 M301 — CH30 M401

OPT. GAIN RES. R106 / R206 / R306 / R406 — E103 / E203 / E303 / E403 — R103 / R203 / R303 / R403 — GAIN RES. R104 / R204 / R304 / R404

SUMMING NODE — LO INPUT — SHIELD INPUT — HI INPUT — PULL UP

PREAMP OUT — POWER DRIVE LO / HI

OFFSET ADJ. R101 / R201 / R301 / R401 50K — R102 / R202 / R302 / R402 270 — C101 / C201 / C301 / C401 1000 pF — GAIN ADJ. R105 / R205 / R305 / R405 200Ω

+5 — 17,4 — +5V PWR — C3 6.8μF — +5 RTN — 16,T — +5V RTN

18,V — +15 V — 19,W — −15V — C1 6.8μF — C2 6.8μF

22,Z — PWR RTN — E10 — E11 — 20,Y

CARD OFFSET — R1 3.4K 1% — R14 1K — R2 23.7K 1% — R3 F.A. — R4 2K 1% — R5 F.A. — R15 2.37K 1% RC4256 DALE — CR1 1N4577 — C4 .01 μF — C5 1000 pF — R6 270 — E8 — E2 — E1

Z1 HA1828A-5 — Z6 74C20 — +5V

A — CARD SELECT — B — C — D

Y — EVEN BUS

2 — 2° — 1 — 2¹ — CH SELECT

21 — ODD BUS

R — SYSTEM CLOCK

Q7 TIS73 — C9 6.8 μF — Q1 Q4 Q2 Q3 2N3904 — 2N3906 — Q6 TIS73 — C8 6.8μF — C10 22μ 35V — C11 2.2μ 35V

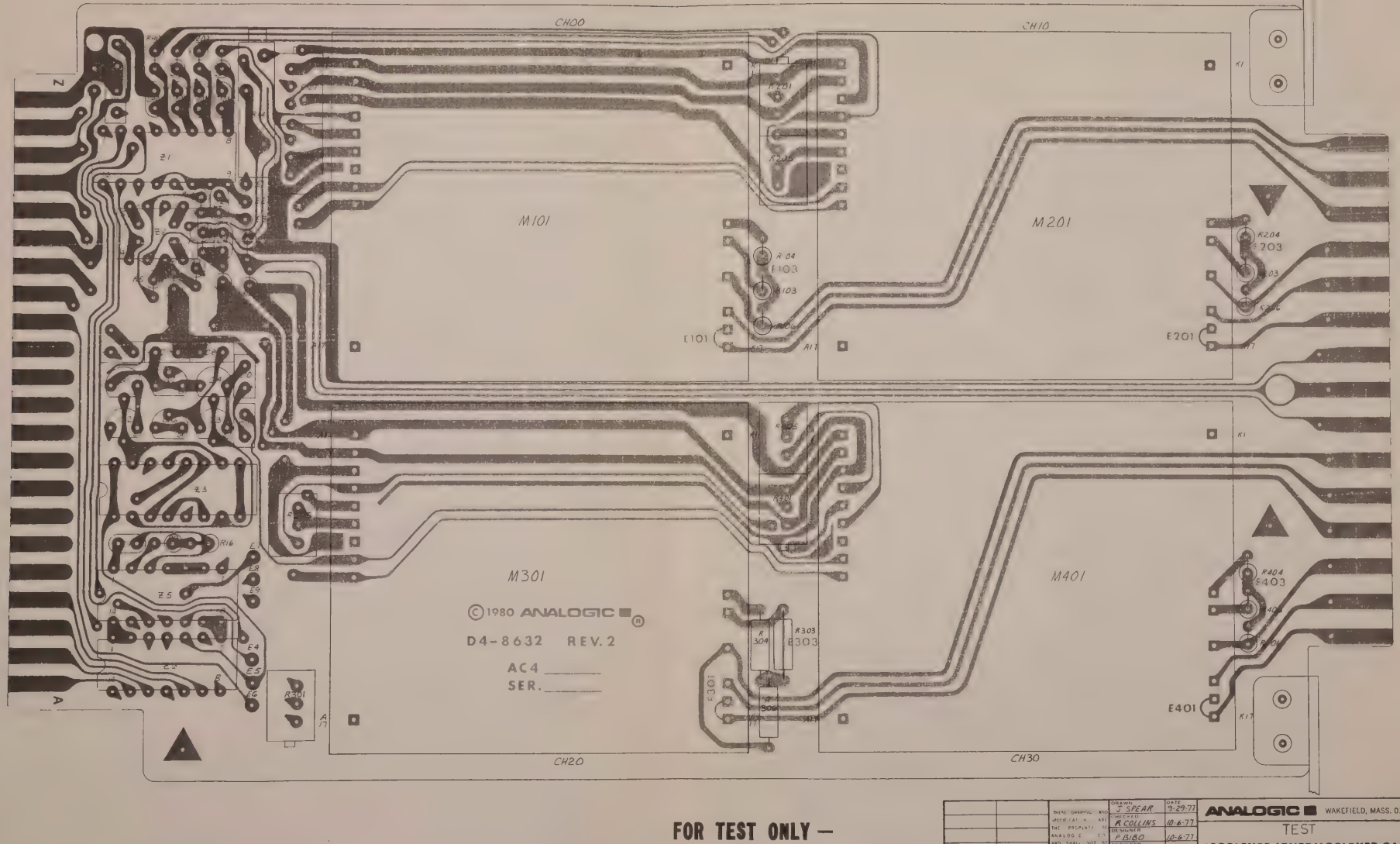
R16 1/A — R9 9.76K — C7 1000pF — Z5 4047 — E4 E5 E6 — Z6 74C20

NOTES:
1) ALL RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
2) QC IS MOUNTED IN CONNECTOR FOR THERMOPLEXER UNITS AC4350→4356 ONLY.
3) —+— DENOTES CUTTABLE ETCH ON WIRING SIDE.
4) SEE P.L. FOR VALUE OF GAIN RESISTORS.

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± DECIMALS ± ANGLES ±	DRAWN	DATE 7/1/77	ANALOGIC ■ WAKEFIELD, MASS. 01880
	CHECKED		AC4050→4054 / AC4350→4256
MATERIAL	ENGINEER	9/29/77	ISOPLEXER / THERMOPLEXER ®
FINISH	APPROVED	9/1/77	
PROD. AC4050→54 / AC4350→56	RELEASED	9/6/77	SIZE IDENT NO. 31814 — SIZE D — 5-8632
NEXT ASSY — USED ON	WEIGHT		SCALE — ACCOUNT NO. — SHEET 1
APPLICATION	APPLICABLE SPECIFICATIONS		


CH00
CH10
CH20
CH30
M101
M201
M301
M401
E101
E201
E401
R 04
E103
R204
E203
R404
E403
R303
E303
R304
E304
R305
E305
R306
E306
R201
R202
R203
R205
R206
R207
R301
R302
R401
R402
R403
R405
R406
R407
Z1
Z3
Z5
R16
E4
E5
E6
E8
E9
A11
A17
K1
K17
A
B
C
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AC4300

BRIDGE TRANSDUCER INPUT CARD FOR ANDS5400

GENERAL DESCRIPTION

The Analogic AC4300 series Bridge Transducer Input Cards provide a flexible, efficient and accurate means for exciting and measuring strain gage devices, pressure sensors, load cells, or RTD bridges within the ANDS5400 system architecture. The AC4300 card is designed to accommodate four separate inputs. Each channel is comprised of an adjustable differential voltage regulator, calibration relay, and chopper-stabilized amplifier. The use of individual amplifiers in each channel ensures excellent performance characteristics and very high system scan rates — up to 100,000 channels per second. The regulation circuits and amplifiers are fully isolated from system ground such that with an external excitation power supply, the four Bridge circuits can operate with up to 200V common-mode potentials.

The AC4380 Bridge Completion Card provides a resistance calibration relay and terminals for completing 1, 2, or 3 arms of each bridge for each channel. It also provides facilities for input of the AC1700 Automatic Offset Compensation Card analog output.

Each AC4300 card occupies a single user slot in the ANDS5400 system; thus, up to 16 cards can be installed in a single enclosure. The AC4380 card fastens to the back of the AC4300 and does not use a slot in the system. Thus, a fully expanded, 8-enclosure, ANDS5400 system is capable of monitoring 512 separate bridge sensors.

The optional AC1700 Automatic Offset Compensation Card provides four floating 16-bit D/A converters which, under computer control, can eliminate offsets caused by large tare loads, mismatched bridge resistors, or sensor drift. The AC1700 is designed to compensate for offsets as large as 10 times the normal signal amplitude when implemented. This card occupies a slot in the system adjacent to the AC4300 card and is cabled to a socket on the AC4380 card.

COMMON AC43XX SPECIFICATIONS

EXCITATION SECTION

Type of Control	Four individual excitation sub-regulators, with differential sense lines, provide accurate control of voltage across each bridge independent of temperature changes, lead length, or power supply drifts. The regulators are controlled by a self-contained precision reference.
Raw Power Supply	13V min., 34V max. These may be obtained from standard ANDS5400 system supply, AN3500 option supply, or from an external dc source. The choice of power source is dictated by the total current drawn by the AC4300 cards and bridges. The raw power must be at least 2 volts greater than the desired bridge voltage plus the voltage drop expected in the wiring to the bridge (if remote).

(continued on next page)

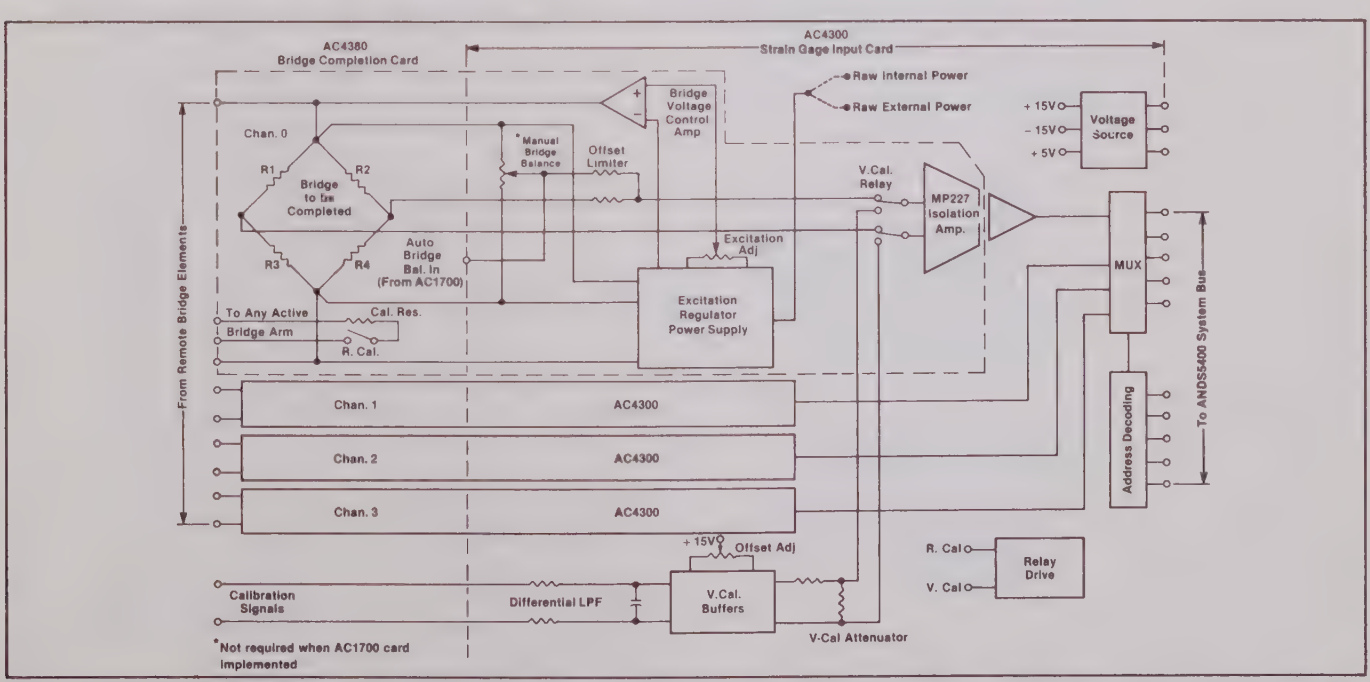

Fig. 1 AC4300 Functional Block Diagram.

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...The Digitizers

COMMON AC43XX SPECIFICATIONS (CONTINUED)

Bridge Voltage Range — 1 to 20V capability. Special considerations are necessary for operation beyond the 6 to 12V range (refer to Excitation Monitoring Capability).

Current Capability — 70mA max., per channel, at any voltage. Each regulator is current-limited at 100mA (25°C). Each output may be short circuited indefinitely when raw excitation supply is 15V or less. Short circuit time reduces to 30 secs., with raw power supply of 30V.

Adjustment Range — Each regulator is pre-configured to deliver a specific voltage, based on the model number of the card. Control potentiometers, on individual regulators, allow for a ±5% adjustment range, for precise setting of bridge voltage.

Stability — For bridge voltages greater than 9 volts: ±25ppm/°C. For bridge voltages less than 9 volts: ±35ppm/°C.

Wiring — Four wires are involved with each bridge excitation: two power wires and two sense wires. Maximum extension distance is 1500 ft. A 6.8μF capacitor should be placed across the bridge supply at the point where the sense lines are connected to the power lines, to optimize transient response. Sense line input resistance = 160k ohms.

Settling Time — 50μsec for settling to 0.01%, after a 50% change in load current.

ISOLATION AMPLIFIER CHARACTERISTICS

Output Voltage — All AC4300 cards are configured to provide a normalized output range of ±10 Volts to the ANDS5400 analog bus.

Gain Range — 50 to 1000, set by factory-installed resistors in each model for desired FS input range.

Gain Accuracy — ±3.5% initial accuracy (can be calibrated by software routine using V-CAL to ±0.02% with a 13-bit A/D converter). Stability: 25ppm/°C. Linearity: 0.01% FSR for gain of 1000; 0.005% FSR for gain of 50 to 500.

Amplifier Offset — Untrimmed, to be removed by system software. ±150μV RTI @ G = 1000; ±600μV RTI @ G = 100.

Input Impedance — 100 megohms. Input bias current = 2nA max.

Filtering — Standard filter: 3-pole with cutoff 6dB down at 5Hz; 60dB per decade beyond 5Hz: Noise: 1μV p-p RTI.

Common-Mode Rejection — Maximum common-mode voltage: ±100Vdc. CMRR: 140dB at 60Hz.

Normal-Mode Input — Maximum 50 volts without damage.

CALIBRATION BUFFERS

Type — Two high impedance buffers follow an externally supplied high-level calibration signal normalized to ±10 volts. The buffer outputs drive an accurate resistive attenuator that produces a signal equal in magnitude to the full scale input of the isolation amplifiers. This attenuated signal is presented to the bridge amplifiers whenever the V-CAL relays are actuated.

Input Impedance — >100 megohms. Bias current <1nA.

Offset Control — Potentiometer control adjusts combined buffer offsets to zero. Stability: ±100μV/°C RTI.

Attenuator — Accuracy: 0.015% FSR. Stability: 15ppm/°C.

BRIDGE BALANCE CONTROL

Type — Either manual or automatic. Manual control consists of a potentiometer for each bridge; this can be adjusted to balance bridges with equal-valued arms that have initial offsets less than ±10% of full scale signal. Automatic control is exercised when the appropriate version of the AC4300 card is mated to the AC4380 and AC1700 cards. With this combination, equal bridge arms are not required and the range of computer-controlled offset can reach 10 times the level of the bridge amplifier full scale input signal.

Stability — 40ppm/°C, referred to full scale range of the isolation amplifier.

OVER-ALL CARD SPECIFICATIONS

Current Drain (with external raw excitation supply) — +15V = 25mA. −15V = 25mA. +5V = 300mA (relays closed).

Current Drain of Excitation Section — 30mA plus current drawn by bridges (310mA max.).

FUNCTIONAL DESCRIPTION

A functional block diagram of the AC4300 Bridge Input Card is shown in Fig. 1. The AC4300 card is capable of exciting and measuring a wide variety of bridges with different bridge voltages and signal magnitudes. Various models of the AC4300 card are tailored to match common bridge networks. The last two digits of the model number indicate exactly which version of the card is being used. (AC4301, AC4302, etc.). Standard cards built by Analogic will always have the same characteristics for all four channels. The AC4300 consists of seven basic sections:

- Amplification Modules
- Calibration Buffers
- Address Decoding
- Excitation Power Supply and Reference
- Relay Drive Circuitry
- Output Multiplexers
- Manual Offset Controls

AMPLIFICATION MODULES

The output of the external transducer, represented by the bridge circuit in Fig. 1, is applied to the input of an MP227 Isolation Amplifier via a Voltage Calibration Relay. The bridge amplifier circuit is factory-configured for a fixed gain of 30mV or 100mV RTI. At his option, the user may configure the amplifier for other gains. The amplifier provides 3-pole (60dB/decade) normal mode filtering from 5Hz; extremely good linearity; high common-mode rejection, (140dB); and is virtually drift-free. Its performance parameters are consistent with systems requiring resolutions of up to 14 bits.

CALIBRATION BUFFERS

External voltage calibration signals are driven to high-input-impedance V-CAL Buffers via a differential low-pass filter. Provision is made in the buffer amplifiers for offset adjustment and attenuation of the calibration signals to compensate for bridge amplifier gain. The calibration signals are passed to the MP227 Isolation Amplifier via the V-CAL Relay when commanded (see Address Decoding).

Manual bridge balancing (AC1700 not implemented) and initial excitation voltage calibration are accomplished, in each channel of the AC4300 card, by individual potentiometers. The amount of offset that can be compensated for by the Bridge Balance control is approximately ±10% of the full-scale signal.

With the AC1700 card implemented, large inherent offsets may be removed by software interaction. It is recommended that an appropriate software program be employed, in conjunction with the voltage and resistance calibration capability, to remove any residual offset or gain errors that may exist in any channel. When used on a weekly basis, such a software routine will produce excellent accuracy without the need for any manual adjustments on the AC4300 card. When the AC1700 card is used for computer-controlled bridge balancing, the system is virtually maintenance-free and provides accuracies far in excess of any system in its class.

ADDRESS DECODING

The address structure of the ANDS5400 provides complete flexibility of configuration and installation. The AC4300 card responds to eight analog addresses and one digital address.

Addressing of Analog Channels

Table 1 details the analog addresses of the AC4300 Bridge Transducer Input Card, installed in any enclosure. A differential range code should always be used when measuring the analog channels. To determine the absolute address of this device, simply add the enclosure analog address to the addresses listed in the Table (see ANDS5400 Manual).

Table 1
ADDRESSING OF ANALOG CHANNELS*

J1	000,004,010,014,020,024,030,034
J2	040,044,050,054,060,064,070,074
J3	100,104,110,114,120,124,130,134
J4	140,144,150,154,160,164,170,174
J5	200,204,210,214,220,224,230,234
J6	240,244,250,254,260,264,270,274
J7	300,304,310,314,320,324,330,334
J8	340,344,350,354,360,364,370,374
J9	400,404,410,414,420,424,430,434
J10	440,444,450,454,460,464,470,474
J11	500,504,510,514,520,524,530,534
J12	540,544,550,554,560,564,570,574
J13	600,604,610,614,620,624,630,634
J14	640,644,650,654,660,664,670,674
J15	700,704,710,714,720,724,730,734
J16	740,744,750,754,760,764,770,774

*See Table 2

Table 2
EXAMPLE OF ANALOG CHANNEL ADDRESSING

ADDRESSES	SIGNAL
0	*Channel 0 Excitation
4	Channel 0 Signal
10	*Channel 1 Excitation
14	Channel 1 Signal
20	*Channel 2 Excitation
24	Channel 2 Signal
30	*Channel 3 Excitation
34	Channel 3 Signal

***Note:** Excitation measurements are only valid if IC Z5 is installed and if the proper limitations on measurement of the excitation voltage have been observed (see Excitation Monitoring Capability).

Addressing of Digital Channels

Table 3 lists the digital addresses of the AC4300 card, installed in any enclosure. To determine the absolute address of this device, simply add the enclosure digital address to the addresses listed in the Table (see ANDS5400 Manual).

Table 3
ADDRESSING OF DIGITAL CHANNELS

J1	0	J9	40
J2	4	J10	44
J3	10	J11	50
J4	14	J12	54
J5	20	J13	60
J6	24	J14	64
J7	30	J15	70
J8	34	J16	74

DIGITAL ADDRESS

A single digital address controls the voltage calibration and resistance calibration relays on the AC4300 and the AC4380 card. This address is equal to the base digital address of the slot in which the AC4300 card is installed.

ADDRESS	DATA BIT MEANING
0	D16 = V-CAL Relay (1 = On)
	D15 = R-CAL Relay (1 = On)

A "one" sent to either bit, in a digital output transaction, closes the associated relays and activates the function. All four relays, associated with either function, operate simultaneously. When the V-CAL relays are closed, the inputs to the MP227 amplifiers are connected to the calibration attenuator; when they are open, the amplifiers are connected to the bridge signals. When the R-CAL relays are closed, the calibration resistor is shunted across one arm of the bridge; when they are open, the bridge functions normally. Special "power up" circuitry on the AC4300 card ensures that all relays are open when the system is turned on. Additional circuitry on the board prevents both sets of relays from being actuated together even if a "one" is sent to both bits in the digital output word. (This is done to limit the total power drain of the card from the 5-volt supply.) If an attempt is made to actuate both sets of relays, only the V-CAL relays will respond.

EXCITATION POWER SUPPLIES

The AC4300 card contains four separate excitation subregulators. These maintain constant voltages across each of the four bridges. The Excitation Adjustment potentiometers provide fine adjustment for each bridge voltage (±5%).

EXCITATION MONITORING CAPABILITY

Individual bridge excitation voltages can be monitored by the ANDS5400 system if IC Z5 is installed in the AC4300 card. The following constraints must be satisfied when Z5 is used:

- The bridge voltage being monitored must be less than the full-scale range of the system A/D converter.
- The magnitude of the voltage on either of the bridge sense lines cannot exceed ±11.5V with respect to system ground.

The above conditions are met when the raw excitation supply is positive with respect to system ground and when the regulated bridge voltages are less than 10 volts.

An expedient may be used to provide monitoring when a negative supply is employed. If the internal System −15V supply is used and if the bridge voltages are below 7V, a dropping resistor or zener diode may be used to raise the minus sense lines above the 11.5V limit.

RELAY DRIVE CIRCUIT

The relay drive circuit operates from the System +5V supply and provides power for both the V-CAL and R-CAL relays. The R-CAL drive circuit may be used to run remoted 5V R-CAL relays. The system 5V power must be used and the total current drain must be less than 200mA. Provision is made in the relay drive circuit to prevent both R-CAL and V-CAL relays from being actuated together. If both relays should be commanded to turn on, only the V-CAL relay will respond.

INPUT MULTIPLEXERS

The AC4300 card output is measured differentially by the ANDS5400 system; in this mode, the even bus acts as the high input to a differential amplifier while the odd bus acts as the low input. When the MP227 amplifier signals are multiplexed to the system bus, the amplifier output becomes the high input to the system and local ground the low input. The common-mode rejection of the system removes any error that may be caused by voltage drops in the system ground lead.

The multiplexer, Z5, monitors the sense leads of each excitation power supply on the AC4300 card as a means of measuring the excitation voltage for each bridge. The plus sense lead is connected to the high input of the system bus and the minus sense lead to the low input.

AC4380 BRIDGE COMPLETION CARD

AC4380 Card Description

The AC4380 Bridge Completion Card is an optional card designed for use with the Analogic AC4300 Bridge Transducer Input Card. It provides the following features:

- Terminals are available for mounting resistors to be used in completing one, two or three arms of the strain gage bridges.
- Relays and resistor mounting terminals are installed which allow activation of the resistor gain calibration function of the AC4300.
- A connector is available that allows plug-in installation of the optional AC1700 bridge balancing card.

The AC4380 is implemented whenever the user wishes to complete certain arms of the bridge near the ANDS5400 System, or when the R-CAL function is to be utilized, or when the AC1700 Card is incorporated in the System. The AC4380 does not occupy a card slot in the ANDS5400, but connects to the back of the AC4300. An integral mechanical bracket assembly supports the AC4380 card and extends the user card connector four inches beyond the rear edge of the chassis. Connections may be made to the AC4380 with the standard AC80 connector assembly furnished with the AC4300 card. Special attention should be given to two areas during installation: One is the additional 4-inch space requirement at the rear of the ANDS5400 chassis; the other is the power dissipation and cooling requirement of the bridge completion resistors. The total power dissipation of the bridge resistors depends on the resistor values and the magnitude of the excitation voltage (power dissipation may approach 1.5 watts per AC4380 card).

System accuracy and stability can be severely compromised by localized self-heating effects on the AC4380 card. Precautions, such as forced air, should be taken to prevent these effects. The card resistors are oriented vertically to promote convective cooling in this critical area. The temperature rise from the bottom to the top of the card should not exceed 2ºC for maximum system accuracy.

The AC4380 is an uncommitted card which does not include any bridge resistors, R-CAL resistors, or any customizing jumpers. To implement the card in a particular application, the user simply installs the appropriate bridge and R-CAL resistors, and solders in the necessary jumpers. The maximum allowable dimensions of the resistors are as follows: Bridge resistors 1" long, 0.40" diam.; R-CAL resistors 0.55" long, 0.25" diam.

Card Installation & Configuration

As an example of a normal installation, it will be assumed that a 350-ohm bridge is to be used in all four channels with three of the arms completed at the AC4380. It will also be assumed that R-CAL is desired and that the internal ANDS5400 supply will be used as a source of the 10V raw excitation voltage.

STEP 1—Examine Drawing D5-6362 (Strain Gage Bridge Completion Techniques), and Drawing D5-8668 (Strain Gage Card Schematic)

STEP 2—Install jumpers

1M—1N 1D—1B	(CHANNEL 0)
2M—2N 2D—2B	(CHANNEL 1)
3M—3N 3D—3B	(CHANNEL 2)
4M—4N 4D—4B	(CHANNEL 3)

STEP 3—Connect pins together on the AC80 connector

2—B 6—F	(CHANNEL 0)
7—H 11—M	(CHANNEL 1)
12—N 16—T	(CHANNEL 2)
17—U 21—Y	(CHANNEL 3)

STEP 4—Connect power jumpers on the AC4380

6—9,
5—8, 10—11 (FOR POWER FROM +15V)

or

6—8,
5—7, 10—13 (FOR POWER FROM −15V)

STEP 5—Install user-supplied bridge resistors

R10, R11,	R13	(CHANNEL 0)
R20, R21	R23	(CHANNEL 1)
R30, R31,	R33	(CHANNEL 2)
R40, R41,	R43	(CHANNEL 3)

STEP 6—Install user-supplied resistance calibration resistors

R14	(CHANNEL 0)
R24	(CHANNEL 1)
R34	(CHANNEL 2)
R44	(CHANNEL 3)

STEP 7—Connect user wiring (three wires per gage) to AC80 connector per example on D5—6362.

PINS B, E, AND 4	(CHANNEL 0)
PINS H, L, AND 9	(CHANNEL 1)
PINS N, S, AND 14	(CHANNEL 2)
PINS U, X, AND 19	(CHANNEL 3)

STEP 8—Connect R-CAL leads to gages

PINS C AND D	(CHANNEL 0)
PINS J AND K	(CHANNEL 1)
PINS P AND R	(CHANNEL 2)
PINS V AND W	(CHANNEL 3)

STEP 9—Connect user calibration source to calibration input of AC80

+V-CAL TO PIN 1
−V-CAL TO PIN A

STEP 10—Attach AC4380 to AC4300, Attach AC80 to AC4380, and verify proper system performance.

AC4300 PIN NUMBERS

+5V	A	1	RLY. CNTL.	
−V-CAL.	B	2	+V-CAL.	
GND.	C	3	GND.	
+ EXCITATION OUT 0	D	4	+ SENSE 0	Chan. 0
(NOT USED)	E	5	+ MEASUREMENT IN 0	
OFFSET 0	F	6	− MEASUREMENT IN 0	
− EXCITATION OUT 0	H	7	− SENSE 0	
+ EXCITATION OUT 1	J	8	+ SENSE 1	Chan. 1
(NOT USED)	K	9	+ MEASUREMENT IN 1	
OFFSET 1	L	10	− MEASUREMENT IN 1	
− EXCITATION OUT 1	M	11	− SENSE 1	
+ EXCITATION OUT 2	N	12	+ SENSE 2	Chan. 2
(NOT USED)	P	13	+ MEASUREMENT IN 2	
OFFSET 2	R	14	− MEASUREMENT IN 2	
− EXCITATION OUT 2	S	15	− SENSE 2	
+ EXCITATION OUT 3	T	16	+ SENSE 3	Chan. 3
(NOT USED)	U	17	+ MEASUREMENT IN 3	
OFFSET 3	V	18	− MEASUREMENT IN 3	
− EXCITATION OUT 3	W	19	− SENSE 3	
GND.	X	20	−V AMP.	
$+V_E$ IN	Y	21	$-V_E$ IN	
+15V OUT	Z	22	−15V OUT	

AC4380 PIN NUMBERS

- V-CAL IN	A	1	+ V-CAL IN	
+ EXCITATION OUT 0	B	2	+ SENSE 0	Chan. 0
R-CAL RESISTOR 0	C	3	− MEASUREMENT IN 0	
R-CAL RELAY 0	D	4	− MEASUREMENT IN 0	
NODE 0	E	5	(NOT USED)	
− EXCITATION OUT 0	F	6	− SENSE 0	
+ EXCITATION OUT 1	H	7	+ SENSE 1	Chan. 1
R-CAL RESISTOR 1	J	8	+ MEASUREMENT IN 1	
R-CAL RELAY 1	K	9	− MEASUREMENT IN 1	
NODE 1	L	10	(NOT USED)	
− EXCITATION OUT 1	M	11	− SENSE 1	
+ EXCITATION OUT 2	N	12	+ SENSE 2	Chan. 2
R-CAL RESISTOR 2	P	13	+ MEASUREMENT IN 2	
R-CAL RELAY 2	R	14	− MEASUREMENT IN 2	
NODE 2	S	15	(NOT USED)	
− EXCITATION OUT 2	T	16	− SENSE 2	
+ EXCITATION OUT 3	U	17	+ SENSE 3	Chan. 3
R-CAL RESISTOR 3	V	18	+ MEASUREMENT IN 3	
R-CAL RELAY 3	W	19	− MEASUREMENT IN 3	
NODE 3	X	20	(NOT USED)	
− EXCITATION OUT 3	Y	21	− SENSE 3	
$+V_E$	Z	22	$-V_E$	

INDIVIDUAL MODEL SPECIFICATIONS

	AC4301	AC4302
Signal Bandwidth	5Hz	5Hz
Bridge Excitation Voltage	10V (5% Adj.)	10V (5% Adj.)
Recommended Raw Excitation Voltage	15 volts	15 volts
Bridge Balance Range	±8.5mV	±3.0mV
Full Scale Signal Magnitude	100mV 3.5% Accuracy	30mV 3.5% Accuracy
Calibration Attenuator	10V in = 100mV out	10V in = 30mV out
Residual Uncompensated Amplifier Offsets	±600μV RTI	±350μV RTI

Please contact the factory for availability of other versions of this device.

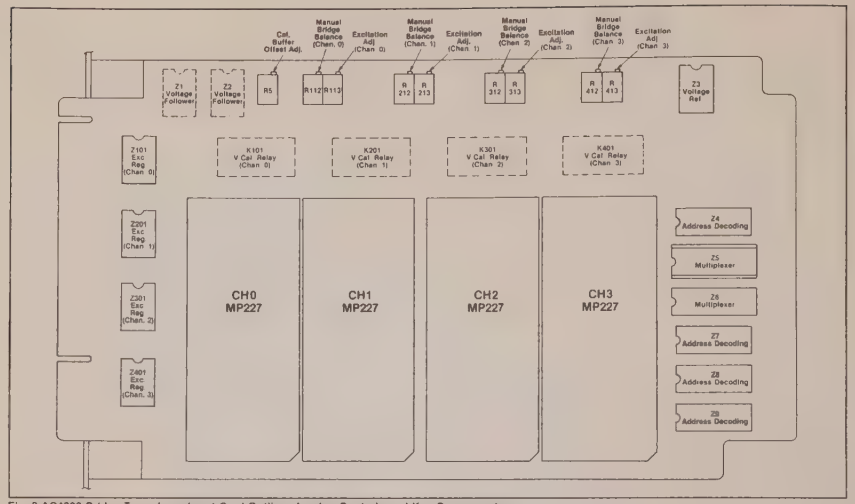

Fig. 2 AC4300 Bridge Transducer Input Card Outline showing Controls and Key Components.

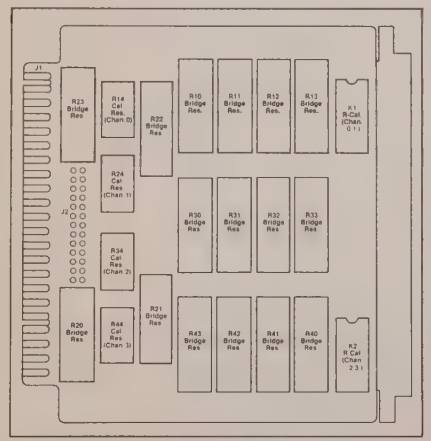

Fig. 3 AC4380 Bridge Completion Card Outline showing Key Components.

IMPLEMENTATION DATA

For calibration and suggested software implementation, see the AC4300 Calibration and Programming procedures and examples presented in a separate data sheet. These procedures include the AC4380 Bridge Completion Card, AC1916 A/D Converter, AC1700 D/A Converter, and specific AC43XX Models.

If additional application assistance should be needed, consult your nearest Analogic sales office or call the factory direct.

ORDERING GUIDE

Simply Specify ..... Enter
For
Bridge Transducer Input Card*
With
100mV FS Output AC4301*
30mV FS Output AC4302*

*Includes AC4380

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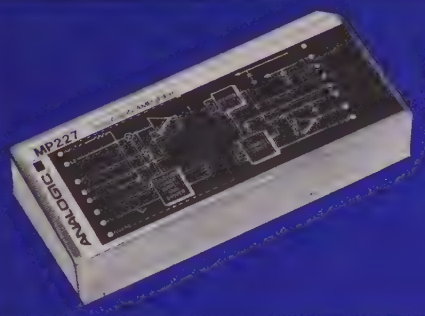

ANALOGIC®

MP227
LOW COST
HIGH PRECISION
ISOLATION AMPLIFIER

DESCRIPTION

The Analogic MP227 is a new precision isolation amplifier which provides an unparalled combination of linearity, stability, isolation, and very low cost. It is designed primarily to replace relays and filter elements in multichannel data acquisition systems. However, its unique features make it attractive wherever low level, low frequency signals must be amplified in the presence of severe common mode interference.

The MP227 offers user-selectable gains from 10 to 1000; input full scale voltage ranges from ±10 mV to ±1 V; 3-pole (60 dB/decade) filtering from 5 Hz; extremely good linearity; superb common-mode rejection; and is virtually drift-free. All parameters are commensurate with A/D conversion at levels up to 14 bits.

The MP227 includes an internal power oscillator and isolated supply so that no external drivers are needed. The isolated power (±4 V nominal) can be used for open thermocouple indication or offsetting strain gage inputs.

APPLICATION

The MP227 was designed as an economically competitive and functionally superior alternative to the relay multiplexing circuits traditionally used in multichannel data acquisition systems. In a typical thermocouple system, the MP227 replaces two functional blocks for each channel; the input filter and a dual relay, as well as the common channel high gain amplifier, and permits high-level, solid-state multiplexing to be used for low cost and reliability.

The MP227 provides significantly better isolation and common mode rejection than low-level relays and it puts the gain at a point in the system where the bandwidth is lowest (prior to multiplexing), thereby reducing total system noise. Even where multiplexing is not used, the unusual combination of performance and price makes the MP227 attractive for a wide variety of industrial instrumentation applications.

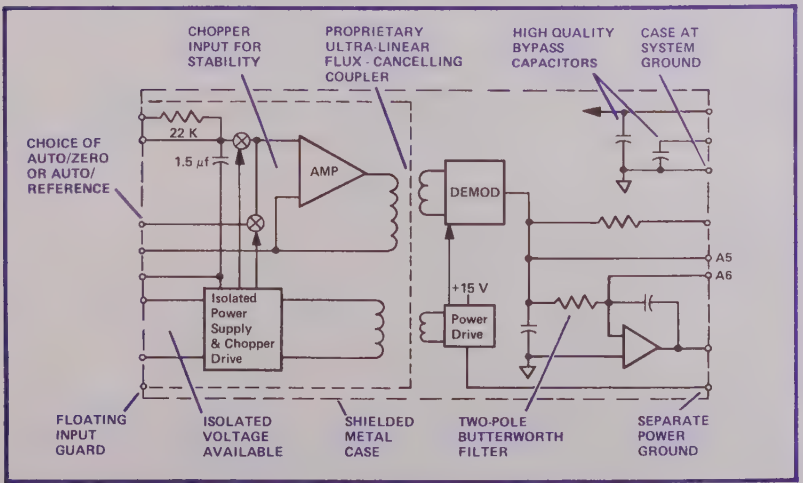

Fig. 1. MP227 Isolation Amplifier Functional Block Diagram.

FEATURES

- Very Low Cost.
- Superior Isolation
  CMRR: 170 dB
  CMV: 1000 V peak.
- Excellent Linearity:
  0.005%.
- Selectable Input Range:
  ±10 mV FS to ±1 V FS.
- Low Noise:
  <0.5 μV RMS.
- Low Drift:
  0.2 μV per °C.
- Low Gain Tempco:
  10 ppm/°C typical.
- Built-In 3-pole Filtering.
- Built-In Oscillator/Driver.

APPLICATIONS

- Thermocouple Temperature Measurements
- Weighing Systems.
- Strain Gage Measurements.
- Remote Data Acquisition and Precision Telemetry Systems.
- Microvolt and Millivolt-Level Measurements.
- Replacement for Classical Differential Amplifier.

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MP227 SPECIFICATIONS

ANALOG INPUT

Gain Range	10 to 1000, non-inverting, resistor programmable. Optimized for gains of 50 to 500.
Nonlinearity	±0.005% FSR Max. @ G = 50 to 500; ±0.01% FSR Max. @ G = 1000; ±0.05% FSR Max. @ G = 10.
Input Amplifier Type	Isolated Chopper.
Linear Differential Input Voltage Range	±10 mV to ±1 V full scale.
Maximum Safe Differential Input Voltage	120 V RMS continuous.
Common Mode Isolation Voltage	1000 VDC, 750 RMS, Max.
Common Mode Rejection Ratio	@ DC and from 50 to 800 Hz: 166 dB Min; 176 dB Typ., @ G = 50 to 1000, 1 kΩ source unbalance.
Common Mode Impedance	10^{10} Ω ‖ 80 pF.
Differential Input Resistance	100 Megohms @ DC.
Differential Input Impedance	See Note 1.
Overload Input Impedance	22 kΩ.
Input Bias Current (See Note 2)	0.5 nA Typ., 2 nA Max.
Offset Voltage, referred to input (RTI)	±150 μV @ G = 1000; ±600 μV @ G = 100, untrimmed. Adjustable to zero.
Voltage Noise (0.01 Hz to 5 Hz)	0.5 μV RMS Max. RTI, 1 μV p-p typical RTI.
Bandwidth (See Note 3)	DC to 5 Hz nominal; 6 dB down @ 5 Hz.
Overall Filtering (See Note 4)	3-pole, 60 dB/decade roll-off (−60 dB @ 50 Hz).
Input Filter	1-pole RC, 3 dB cut-off @ 5 Hz.
Output Filter	2-pole Butterworth, 3 dB cut-off @ 5 Hz.

ANALOG OUTPUT

Voltage Range	±10 V full scale.
Output Impedance @ DC	0.1 Ω.
Maximum Load	±5 mA and 500 pF.
Output Protection	Continuous short-circuit to ground.
Output Chopper Noise 1 MHz Bandwidth	1 mV p-p spike at approximately 7 kHz. See Note 5.

STABILITY

Gain Tempco @ G = 10 to 500	±10 ppm FSR/°C Typ., ±20 ppm FSR/°C Max.
Gain Tempco @ G = 1000	±20 ppm FSR/°C Typ., ±30 ppm FSR/°C Max.
Offset Voltage Tempco	0.2 μV/°C Typ., RTI, 0.5 μV/°C Max. RTI.
Bias Current Tempco	50 pA/°C.
Power Supply sensitivity	±2 μV/% change in supply voltages RTI.
Warm up Drift (5 minutes)	<2 μV RTI.
Long Term Drift	1 μV/month RTI, non-cumulative, 2 μV/year.

ISOLATED POWER SUPPLY OUTPUT

Voltage	±4 VDC Nominal, with respect to input LO.
Current	±3 mA Full load.
Regulation	6%, no load to full load.
Ripple	20 mV p-p; @ 7 kHz.

INPUT POWER SUPPLY REQUIREMENTS

Positive Supply	+15 V, ±3% @ 5 mA, no load.
Negative Supply	−15 V ±3% @ −3 mA, no load.

ENVIRONMENTAL AND PACKAGING

Rated Performance Temperature Range	0 to +70°C.
Operating Temperature Range	−25°C to +85°C.
Storage Temperature Range	−55°C to +85°C.
Relative Humidity	0 to 85%, non-condensing to +40°C.
Dimensions	30 x 70 x 12 mm, 1.2 x 2.8 x 0.5 in.
Shielding	RFI: 6 sides, EMI: 5 sides.

Note 1:	100 Megohms shunted by series combination of 22 kΩ and 1.5 μF. See Fig. 1.
Note 2:	Modified by open input indicator, if used.
Note 3:	Other bandwidths are available, on large quantity orders, from DC to 100 Hz.
Note 4:	Filter nodes externally accessible to allow modification of characteristics.
Note 5:	Can be reduced to negligible level by suggested output multiplexer circuit.

OPERATION AND ADJUSTMENT

OFFSET ADJUSTMENT

Provision is made for external offset adjustment on the MP227 Precision Isolation Amplifier, by connecting a 25 k or 50 k-ohm (100 PPM/°C or better) multi-turn poteniometer (R2) plus a 1 Megohm resistor as shown in Fig. 2. To adjust, momentarily short INPUT HI, INPUT LO, and AZ RTN to the output ANA RTN and set the offset potentiometer for zero output at the OUTPUT terminal.

SETTING THE MP227 GAIN

The gain of the MP227 may be set to any value from 10 to 1000 by connecting an external resistor (R_G) between the GAIN terminal and the INPUT LO terminal as shown in Fig. 2. Gain = $\frac{10^4}{R_G}$

An RN55E (or better) resistor is recommended for temperature stability. Untrimmed, the absolute gain will be within 3% of the calculated value.

GAIN TRIMMING

The gain may be deliberately fine-trimmed, if desired, by connecting a 500-ohm (100 PPM/°C or better) potentiometer (R1) between the FEEDBACK terminal and OUTPUT terminal as shown in Fig. 2. R1 compensates for the tolerance of R_G plus the unit-to-unit gain variability (3%) between multiple MP227's. This also allows standarization of the outputs of multiple MP227's to a common full scale range. For volume production where cost is a factor, the trimpot may be replaced with a fixed resistor selected during final test.

AUTO-ZERO RETURN

The signal that is amplified by the MP227 is actually the difference between the INPUT HI and the Auto-Zero (AZ) voltages. For normal operation, tie the AZ terminal directly to the INPUT LO terminal. In some applications, it may be convenient to offset the input deliberately by an amount that exceeds the range of the OFFSET trimpot (for example, to obtain expanded scale operation or to cancel out the initial or "tare" output of a load cell). To do this, connect the AZ terminal to a stable source of voltage equal to the desired offset.

Observe that both the INPUT HI signal and the AZ signal (if any) are measured with respect to the INPUT LO terminal. For best linearity, each signal must be within ±1 volt of INPUT LO.

OPEN INPUT INDICATION

The user-accessible isolated power supply voltages make it possible to use a simple open input indication network. Connect a resistor on the order of 180 megohms to the INPUT HI and either the +4 volt or –4 volt terminal. This network produces a bleeder current of approximately 20 nanoamps through the input source circuitry. If the source should open, this bleeder current will drive the MP227 output into a saturated state. The speed of this response is a function of the MP227 gain setting and input time constant.

MULTIPLEXING MP227's

The outputs of multiple MP227's may be multiplexed to a common analog line as indicated in Fig. 3. A single RC filter ahead of each MUX input is suggested. See Application Note No. 350 for details.

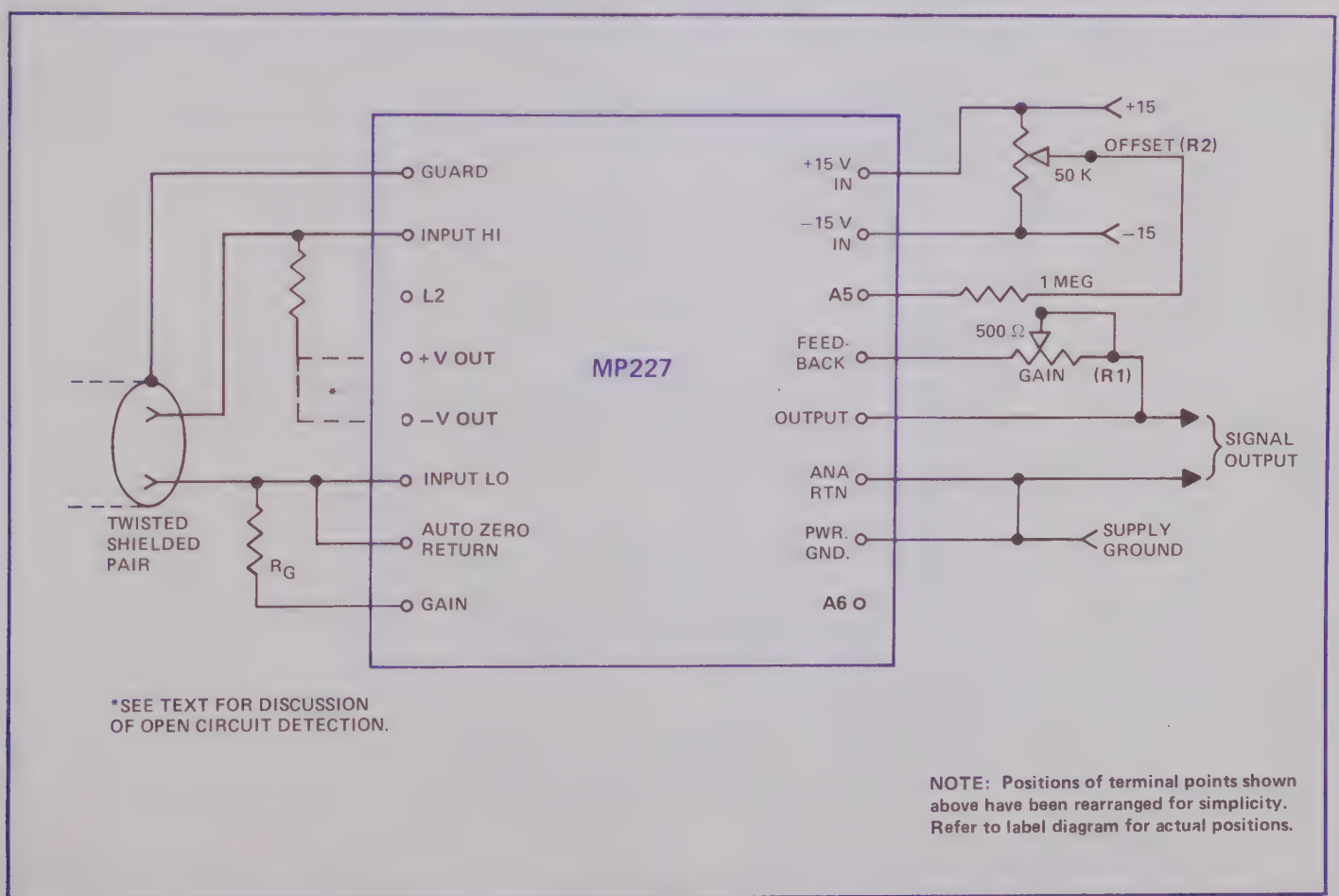

Fig. 2. Typical External Connections MP227.

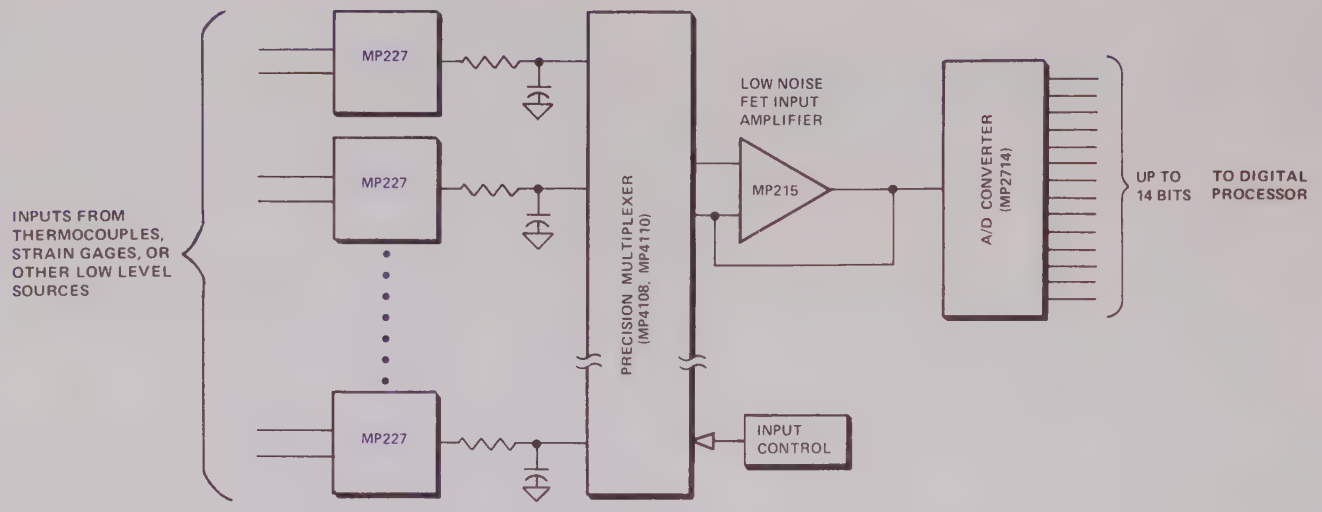

Fig. 3. Multiplexing Diagram, MP227.

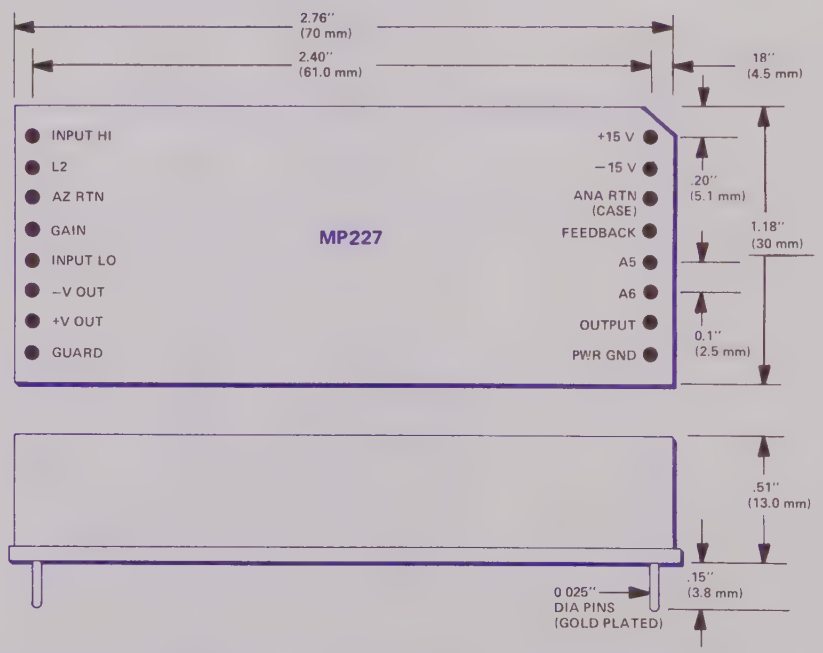

Fig. 4. Outline Mechanical.

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ANALOGIC AG ■ Kanalstrasse 15 ■ Postfach CH-8152 ■ Glattbrugg ■ Switzerland
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ANALOGIC LIMITED ■ 68 High Street ■ Weybridge, Surrey KT13 8BN ■ England
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BRIDGE COMPLETION CARD (FOR REF. ONLY)

STRAIN GAGE INPUT CARD

CHANNEL Ø

CHAN 1

CHAN 2

CHAN 3

NOTE: M1 SWITCH CONTACTS 1,7 - CHAN Ø; 8,14 - CHAN 1
M2 SWITCH CONTACTS 1,7 - CHAN 2; 8,14 - CHAN 3

74C08 SPARES

N.C.

AC4380 PINOUTS

AC43XX PINOUTS

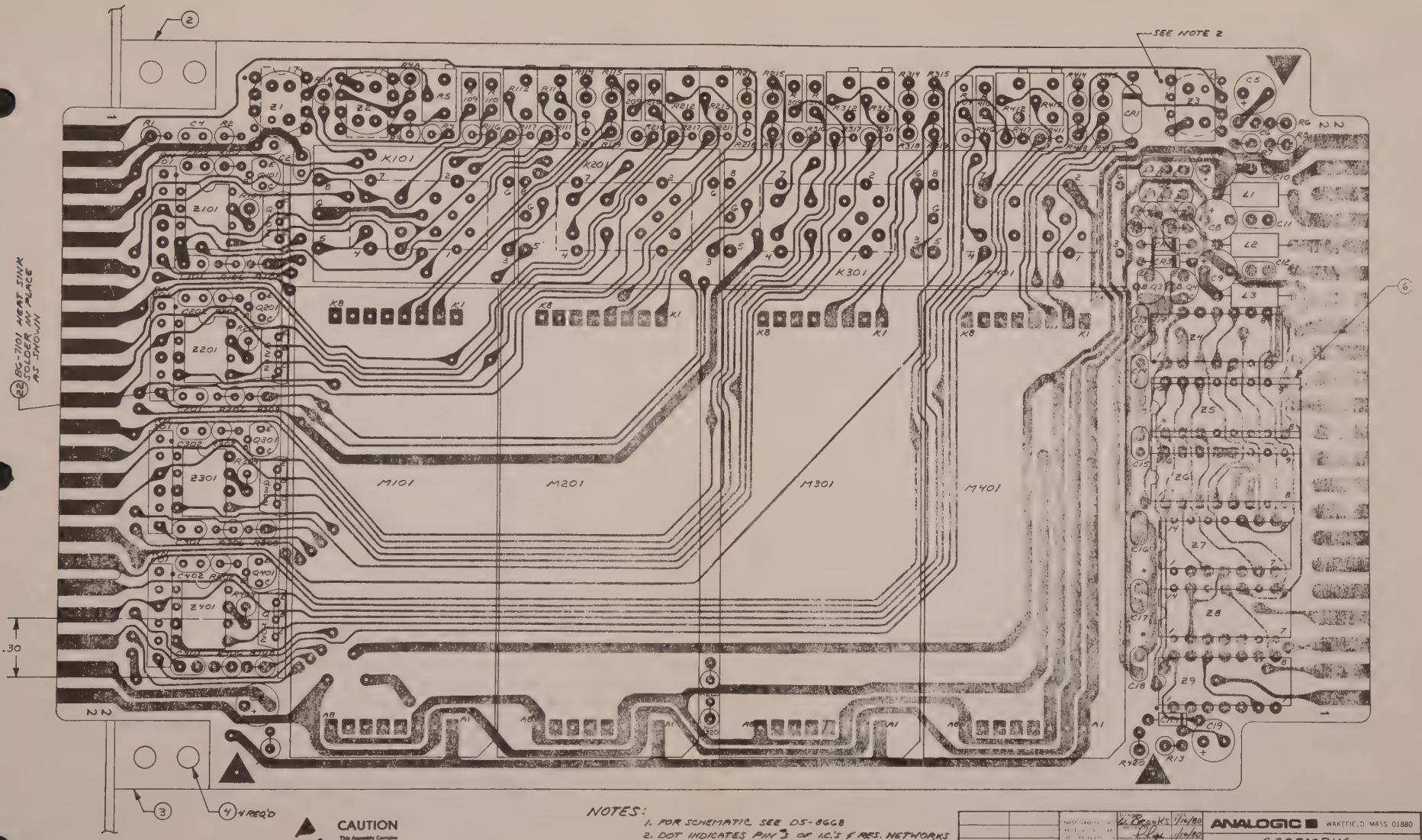
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
2		ENG UPDATE	EE		1-14-80

PL10-8668	AC 43XX	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: DECIMALS .XX ± .XXX, ANGLES ±	DRAWN	DATE 12-17-79
NEXT ASSY	USED ON	APPLICABLE SPECIFICATIONS	CHECKED	1/14/80
APPLICATION		MATERIAL	ENGINEER	1-22-80
		FINISH	ENGINEERING MGR	1-22-80
			QUALITY CONTROL	1-22-80
			PRODUCTION	1-22-80
			WEIGHT	

ANALOGIC, WAKEFIELD, MASS. 01880

SCHEMATIC
STRAIN GAGE CARD
AC-43XX

CODE IDENT NO.	SIZE		REV
31814	D	5-8668	2
SCALE NONE		SHEET 1 OF 1	



NOTES:
1. FOR SCHEMATIC SEE DS-8668
2. DOT INDICATES PIN 1 OF 10.5 & RES. NETWORKS
3. ASSEMBLE PER A2-1027
4. MAXIMUM COMPONENT HEIGHT TO BE .530".

CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.

COMPONENT SIDE

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
2	—	ENG UPDATE	RR		1-6-80

			W. Brooks	1/4/80
				1/4/80
				1-23-80
				1-22-80
				1-22-80
				1-22-80
PL10-8668	AC-43XX			
NEXT ASSY	USED ON			
APPLICATION				

ANALOGIC WAKEFIELD MASS 01880

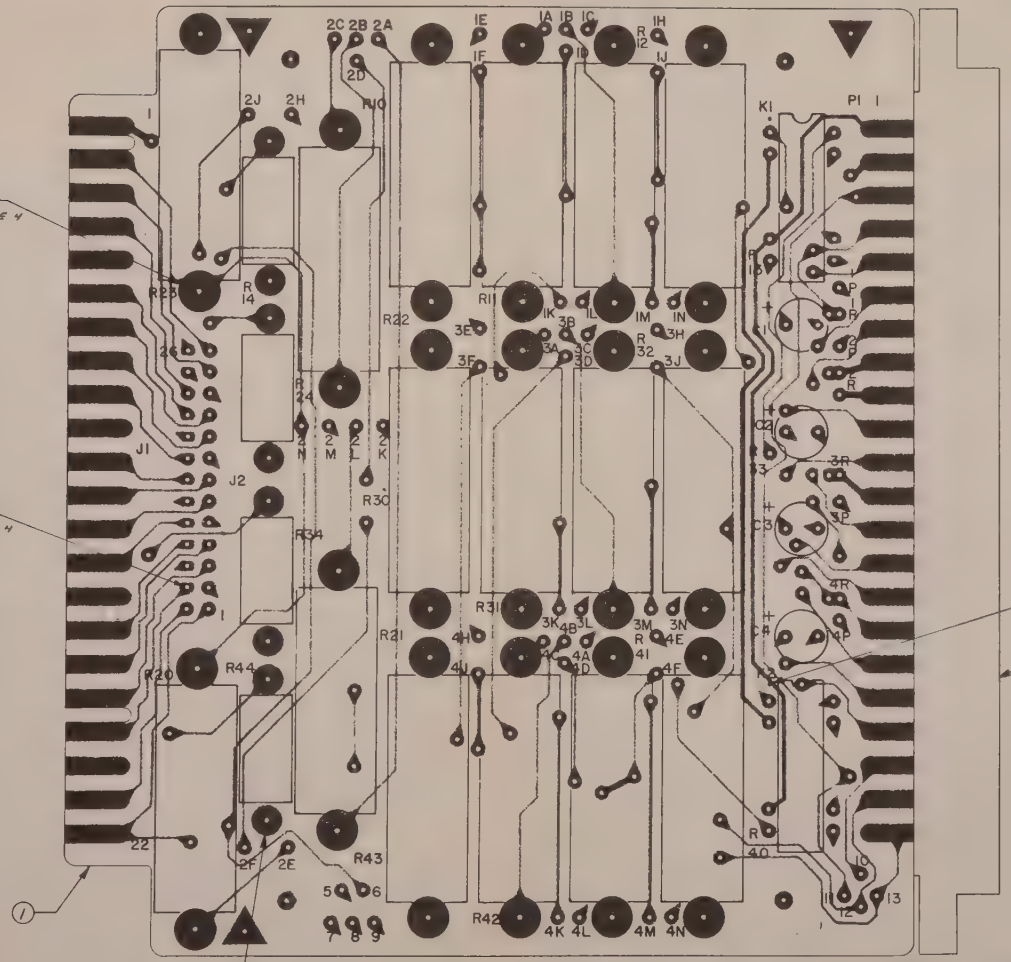
ASSEMBLY
STRAIN GAGE CARD
AC43XX

SIZE	DWG NO	REV
D	7-8668	2
SCALE 4:1	ACCOUNT NO	SHEET 1 OF 1

31814

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
A	-	ENG. UPDATE			

SIZE D — 7-8672 — REV 1



COMPONENT SIDE

NOTES:

1. FOR SCHEMATIC SEE D5-8672
2. DOT INDICATES PIN #1 OF RELAYS
3. ASSEMBLE PER A2-1027
4. INSTALL PRIOR TO WAVE SOLDER
5. MAXIMUM COMPONENT HEIGHT TO BE .510"

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: DECIMALS ANGLES .X ± .03 ± XXX ±	DRAWN E.L. Brooks	DATE 7/15/80	ANALOGIC, WAKEFIELD, MASS. 01880
			CHECKED J. Kelly	11/21/80	ASSEMBLY BRIDGE COMPLETION BD. AC 4330
		MATERIAL	ENGINEER N/A	1-22-80	
		FINISH	ENGINEERING MGR. [illegible]	1-22-80	
PL10-8672	AC 4330	APPLICABLE SPECIFICATIONS	QUALITY CONTROL [illegible]	1-22-80	CODE IDENT NO 31814 — SIZE D — 7-8672 — REV 1
NEXT ASSY	USED ON		PRODUCTION [illegible]	1-22-80	SCALE 4/1 — SHEET 1 OF 1
APPLICATION			WEIGHT		

AC4720

HIGH LEVEL SINGLE-ENDED / DIFFERENTIAL MULTIPLEXER FOR AN5400

GENERAL

The AC4720 Multiplexer card transfers either 32 Single-ended or 16 Differential channels of input signals, under program control of the AN5400 system user. Each channel is independently protected against applied overvoltages (up to 25 volts). See specifications for overvoltage protection details.

Crosstalk between channels is attenuated by over 80dB at dc and by over 60dB at 60Hz. Channel addressing and programming for either single-ended or differential input configuration are described in Chapters 3 and 5 of the AN5400 Instruction Manual and in the data sheet for the installed interface unit.

NOTE: The AC4720 requires no calibration.

AC4720 PERFORMANCE SPECIFICATIONS

Input Impedance:	>100M ohms
On channel leakage current:	<100nA
Offset voltage:	0.25mV (MAX)
Transfer accuracy:	0.01%
Settling time to .02%FSR:	6μS (with 470pF bus load capacitance) (MAX)
Crosstalk:	81dB @ DC 74dB @ 6Hz 63dB @ 60Hz
Input voltage range (signal plus common mode):	±11 volts
Overvoltage:	±25 volts all inputs 10% duty. (Power on) ±21 volts one input continuous duty. (Power on) ±11 volts continuous. (Power off).

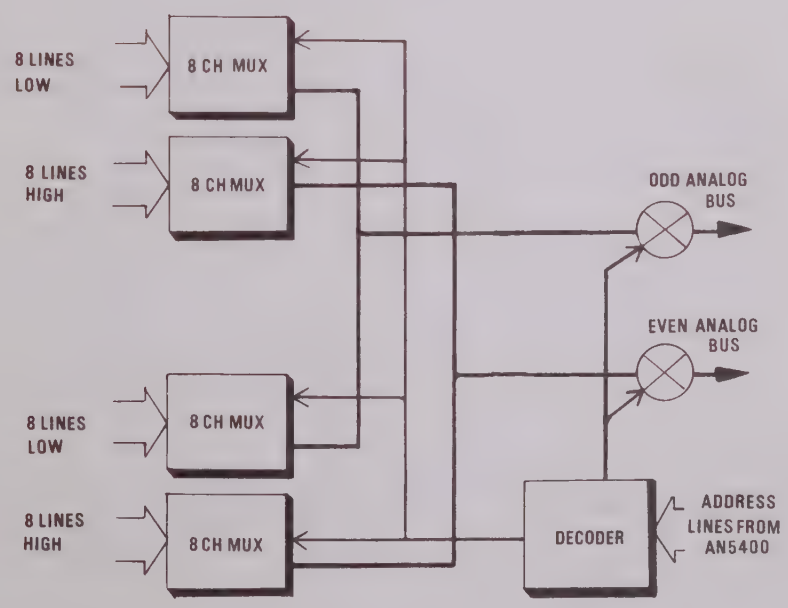


Fig. 1. AC4720 Simplified Block Diagram.

PIN CONNECTIONS (user)

Signal RTRN	A	1	
ANALOG GND	B	2	ANALOG GND
* Input Channels High (EVEN) 0	C	3	1
2	D	4	3
4	E	5	5
6	F	6	7
10	H	7	11
12	J	8	13
			Input Channels Low (ODD)
ANALOG GND	K	9	ANALOG GND
Input Channels High (EVEN) 14	L	10	15
16	M	11	17
20	N	12	21
22	P	13	23
			Input Channels Low (ODD)
ANALOG GND	R	14	ANALOG GND
Input Channels High (EVEN) 24	S	15	25
26	T	16	27
30	U	17	31
32	V	18	33
34	W	19	35
36	X	20	37
			Input Channels Low (ODD)
ANALOG GND	Y	21	ANALOG GND
	Z	22	Signal RTRN

* Differential Input channels are configured by respective pairs. For example: 0 & 1, 2 & 3. 4 & 5, etc.

NOTE:
The Signal RTRN line available on pins A and 22 is used for pseudo-differential operation as described in the signal processor data sheet. If this feature is not used, the signal return line must be connected to ANALOG GND on at least one user card for proper system operation.

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AC4730 SERIES

HIGH LEVEL FILTER MULTIPLEXER FOR AN5400

GENERAL

The AC4730 Series Multiplexer card conditions 16 channels of differential input signals with a 2-pole RC filter. The user may choose any one of four corner frequencies for the filtering action; refer to the Specifications to specify the appropriate card in this series for the desired pass band.

Each card in this Multiplexer series provides overvoltage protection up to 25 volts on all channels of the card, whether or not power is applied. Crosstalk between channels is attenuated by over 80dB at dc and over 60dB at 60Hz. Channel addressing is described in Chapters 3 and 5 of the AN5400 Instruction Manual and in the data sheet for the installed interface unit.

Figure 1 is a block diagram of the cards in this series, and Figure 2 illustrates the signal conditioner schematic.

AC473X PERFORMANCE SPECIFICATIONS

Input Impedance:	>100M ohms
On channel leakage current:	<100nA
Offset voltage Range:	Adjustable ±20mV
Transfer Accuracy:	0.01% @ DC
Filter Roll off:	40dB/decade
Corner frequency:	AC4730 = 10dB @ 12Hz AC4731 = 10dB @ 100Hz AC4732 = 10dB @ 1kHz AC4733 = 10dB @ 10kHz
Crosstalk:	81dB @ DC 63dB @ 60Hz
Input voltage range (signal plus common mode):	±11 volts
Overvoltage:	±25 volts all inputs continuous. (Power on or off)

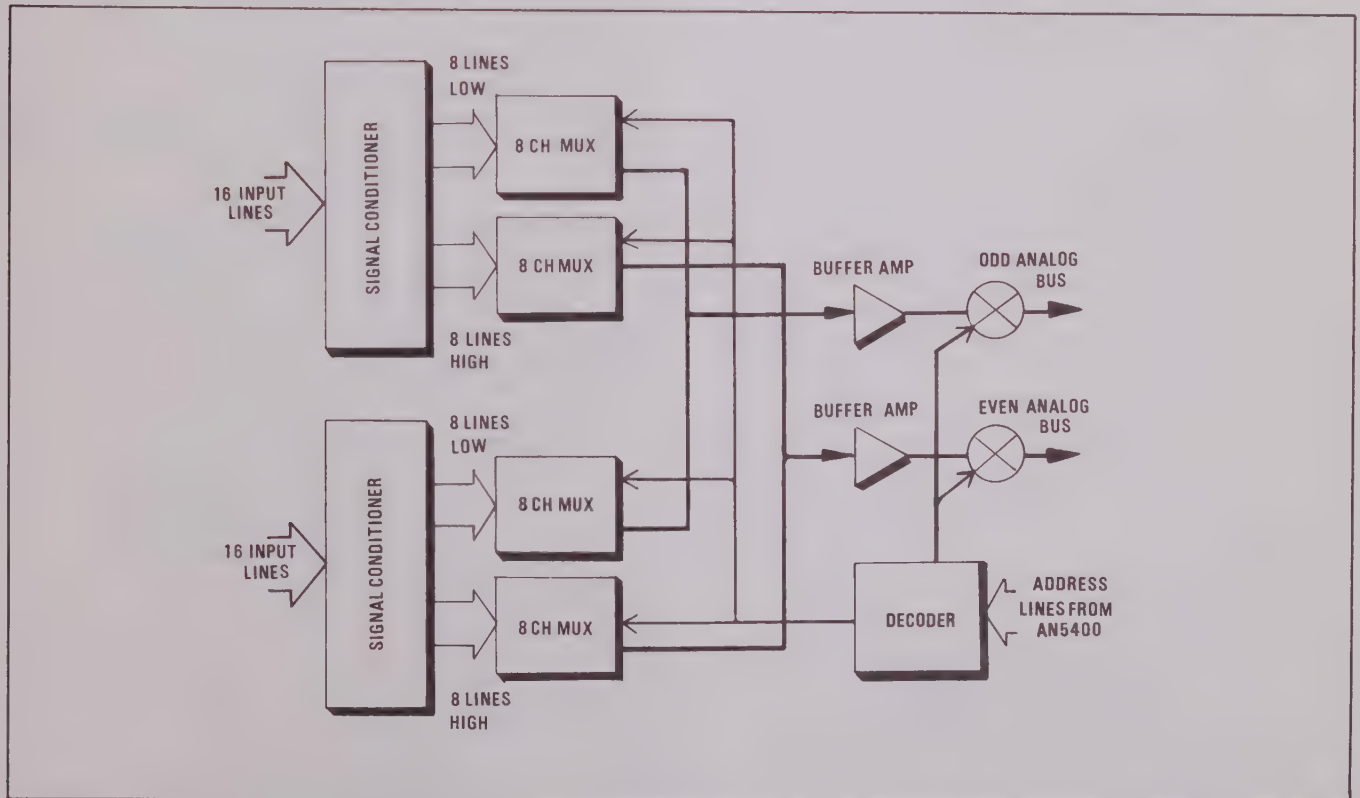

Fig. 1. AC4730 Series Simplified Block Diagram

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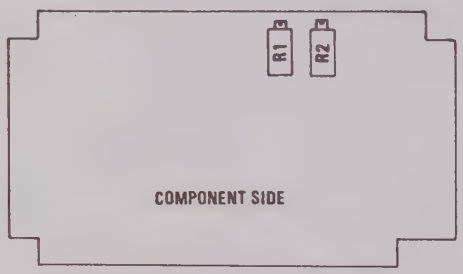
CALIBRATION

Before adjusting offset, make sure offset and range have been adjusted on the A/D converter and signal processor. Short all inputs to signal return and provide a path from signal return to analog ground. Load the code for maximum gain into the front panel range register and an **EVEN** address on the address register following procedures detailed in chapter 3 of the AN5400 manual. Adjust potentiometer R1 for a code of 000000 on the A/D output. Select an **ODD** address and adjust potentiometer R2 for zero code.



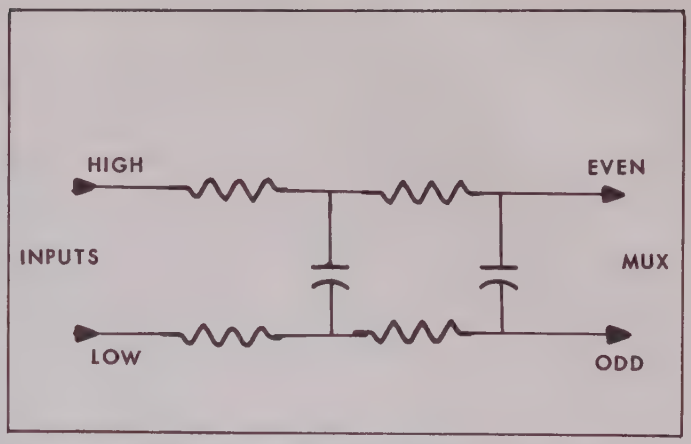


Fig. 2. AC4730 Series Input Signal Conditioner Schematic

PIN CONNECTIONS (user)

Signal RTRN	A	1	
ANALOG GND	B	2	ANALOG GND
* Input Channels High (EVEN) 0	C	3	1
2	D	4	3
4	E	5	5
6	F	6	7
10	H	7	11
12	J	8	13
			Input Channels Low (ODD)
ANALOG GND	K	9	ANALOG GND
Input Channels High (EVEN) 14	L	10	15
16	M	11	17
20	N	12	21
22	P	13	23
			Input Channels Low (ODD)
ANALOG GND	R	14	ANALOG GND
Input Channels High (EVEN) 24	S	15	25
26	T	16	27
30	U	17	31
32	V	18	33
34	W	19	35
36	X	20	37
			Input Channels Low (ODD)
ANALOG GND	Y	21	ANALOG GND
	Z	22	Signal RTRN

* Differential Input channels are configured by respective pairs. For example: 0 & 1, 2 & 3. 4 & 5, etc.

NOTE:
The **Signal RTRN** line available on pins A and 22 is used for pseudo-differential operation as described in the signal processor data sheet. If this feature is not used, the signal return line must be connected to **ANALOG GND** on at least one user card for proper system operation.

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AC4740

DIFFERENTIAL INPUT CURRENT (0-50 MA) MULTIPLEXER FOR AN5400

GENERAL

The AC4740 multiplexer card transfers 16 channels of differential input current (0 - 50mA) signals, under program control of the AN5400 System. Each channel is protected against applied voltages up to 25 volts.

Crosstalk between channels is attenuated by over 80dB at dc and by over 60dB at 60Hz. Channel addressing is described in Chapters 3 and 5 of the AN5400 Instruction Manual and in the data sheet for the installed interface unit.

Figure 1 is a block diagram of the AC4740 and Figure 2 illustrates one section of the signal conditioner circuit.

NOTE: The AC4740 requires no calibration.

AC4740 PERFORMANCE SPECIFICATIONS

Input Impedance:	62.5Ω ± .05% (current input)
Output offset voltage:	<0.25mV
Full scale current:	±50mA
Common mode voltage range:	±8 volts
Transfer accuracy:	±0.05%
Tempco of transfer accuracy:	20ppm/°C
Common mode voltage rejection:	75dB @DC
Crosstalk:	81dB @ DC 63dB @ 60Hz
Overvoltage:	±25 volts all inputs, 10% duty. (Power on) ±21 volts one input, continuous duty (Power on) ±11 volts continuous. (Power off)
Overcurrent:	±100 mA maximum

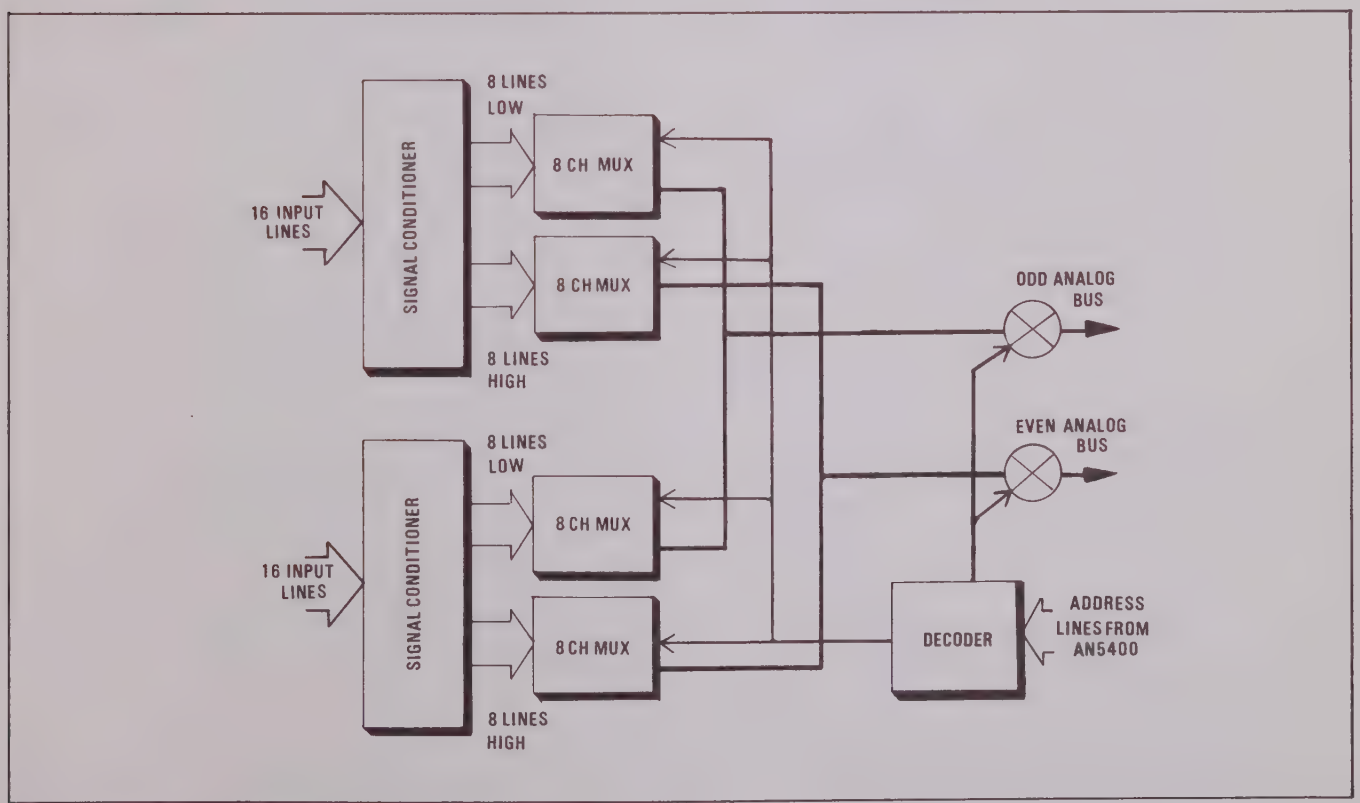

Fig. 1. AC4740 Simplified Block Diagram

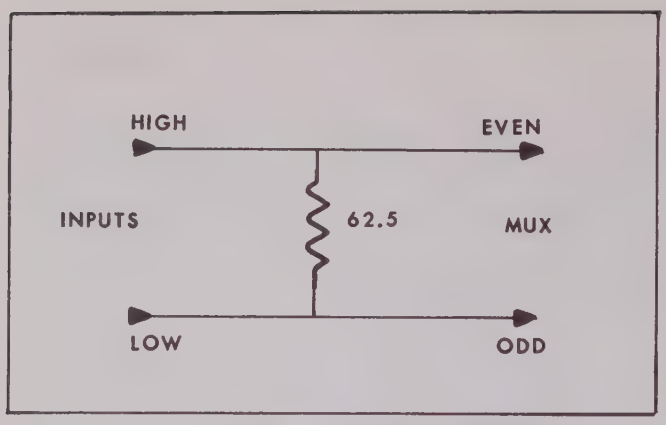

Fig. 2. AC4740 Input Signal Conditioner Schematic

PIN CONNECTIONS (user)

Signal RTRN	A	1	
ANALOG GND	B	2	ANALOG GND
* Input Channels High (EVEN) 0	C	3	1
2	D	4	3
4	E	5	5 — Input Channels Low (ODD)
6	F	6	7
10	H	7	11
12	J	8	13
ANALOG GND	K	9	ANALOG GND
Input Channels High (EVEN) 14	L	10	15
16	M	11	17 — Input Channels Low (ODD)
20	N	12	21
22	P	13	23
ANALOG GND	R	14	ANALOG GND
Input Channels High (EVEN) 24	S	15	25
26	T	16	27
30	U	17	31 — Input Channels Low (ODD)
32	V	18	33
34	W	19	35
36	X	20	37
ANALOG GND	Y	21	ANALOG GND
	Z	22	Signal RTRN

* Differential Input channels are configured by respective pairs. For example: 0 & 1, 2 & 3. 4 & 5, etc.

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AC4750 SERIES

HIGH LEVEL ATTENUATOR MULTIPLEXER FOR AN5400

GENERAL

The AC4750 Series Multiplexer card conditions 16 channels of single-ended input signals by an attenuation factor of 2, 3, 4, 5, or 10. Refer to the Specifications to specify the particular AC4750 for the desired attenuation.

Each card of this Multiplexer series provides overvoltage protection up to 25 volts on all ODD channels, whether or not power is applied. Overvoltage protection for EVEN channels is detailed in the performance specifications. Crosstalk between channels is attenuated by more than 80dB at dc and over 60dB at 60Hz. Channel addressing is described in Chapters 3 and 5 of the AN5400 Instruction Manual and in the data sheet for the installed interface unit.

Figure 1 is a block diagram of the cards in this series, and Figure 2 illustrates one section of the signal conditioner schematic.

NOTE: The AC475X is single ended only, low side inputs (odd) should be connected to signal return. The card output should be measured differentially by the AN5400 to eliminate ground drop errors.

AC475X PERFORMANCE SPECIFICATION

Transfer Accuracy:	0.02%
Tempco of Accuracy	5ppm/°C
Leakage current:	<50nA
Settling time (to 0.01% FSR):	5μS (with 470pf bus load capacitance)
Offset range:	Adjustable ±20mV
Crosstalk:	81dB @ DC 63dB @ 60hZ
Overvoltage, odd inputs:	±25 volts continuous
Input Impedance:	AC4750 = 20KΩ AC4751 = 22.5KΩ AC4752 = 26.6KΩ AC4753 = 31.25KΩ AC4754 = 50.6KΩ
Input Attenuation:	AC4750 = 2 AC4751 = 3 AC4752 = 4 AC4753 = 5 AC4754 = 10
Full scale voltage range:	AC4750 = ±20V AC4751 = ±30V AC4752 = ±40V AC4753 = ±50V AC4754 = ±100V
Overvoltage (all even inputs, continuous):	AC4750 = ±50V AC4751 = ±60V AC4752 = ±80V AC4753 = ±100V AC4754 = ±150V

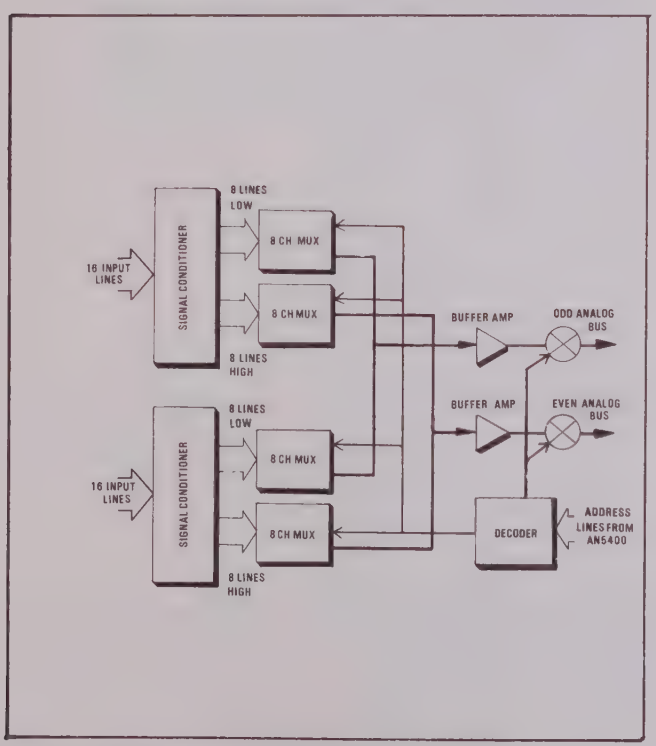


Fig. 1. AC4750 Series Simplified Block Diagram

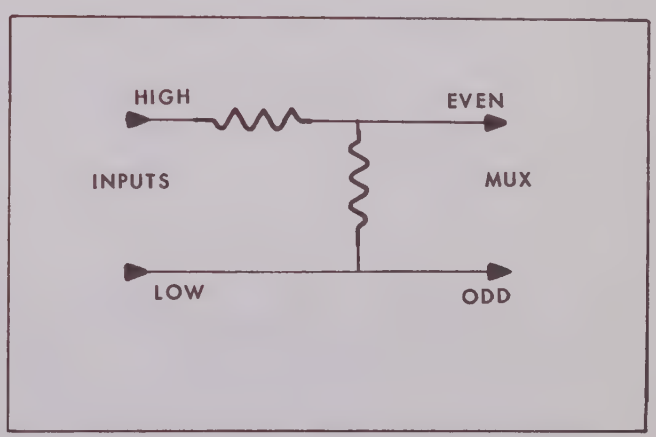
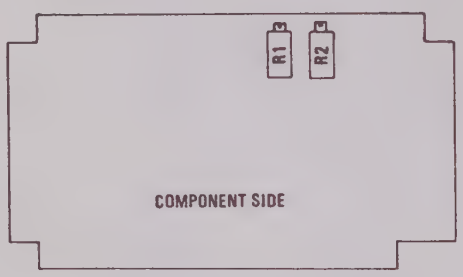


Fig. 2. AC4750 Series Input Signal Conditioner Schematic

CALIBRATION

Before adjusting offset, make sure offset and range have been adjusted on the A/D converter and signal processor. Short all inputs to signal return and provide a path from signal return to analog ground. Load the code for maximum gain into the front panel range register and an **EVEN** address on the address register following procedures detailed in chapter 3 of the AN5400 manual. Adjust potentiometer R1 for a code of 000000 on the A/D output. Select an **ODD** address and adjust potentiometer R2 for zero code.



PIN CONNECTIONS (user)

Signal RTRN	A	1	
ANALOG GND	B	2	ANALOG GND
* Input Channels High (EVEN) 0	C	3	1
2	D	4	3
4	E	5	5 — Input Channels Low (ODD)
6	F	6	7
10	H	7	11
12	J	8	13
ANALOG GND	K	9	ANALOG GND
Input Channels High (EVEN) 14	L	10	15
16	M	11	17 — Input Channels Low (ODD)
20	N	12	21
22	P	13	23
ANALOG GND	R	14	ANALOG GND
Input Channels High (EVEN) 24	S	15	25
26	T	16	27
30	U	17	31 — Input Channels Low (ODD)
32	V	18	33
34	W	19	35
36	X	20	37
ANALOG GND	Y	21	ANALOG GND
	Z	22	Signal RTRN

* Differential Input channels are configured by respective pairs. For example: 0 & 1, 2 & 3. 4 & 5, etc.

NOTE:
The **Signal RTRN** line available on pins A and 22 is used for pseudo-differential operation as described in the signal processor data sheet. If this feature is not used, the signal return line must be connected to **ANALOG GND** on at least one user card for proper system operation.

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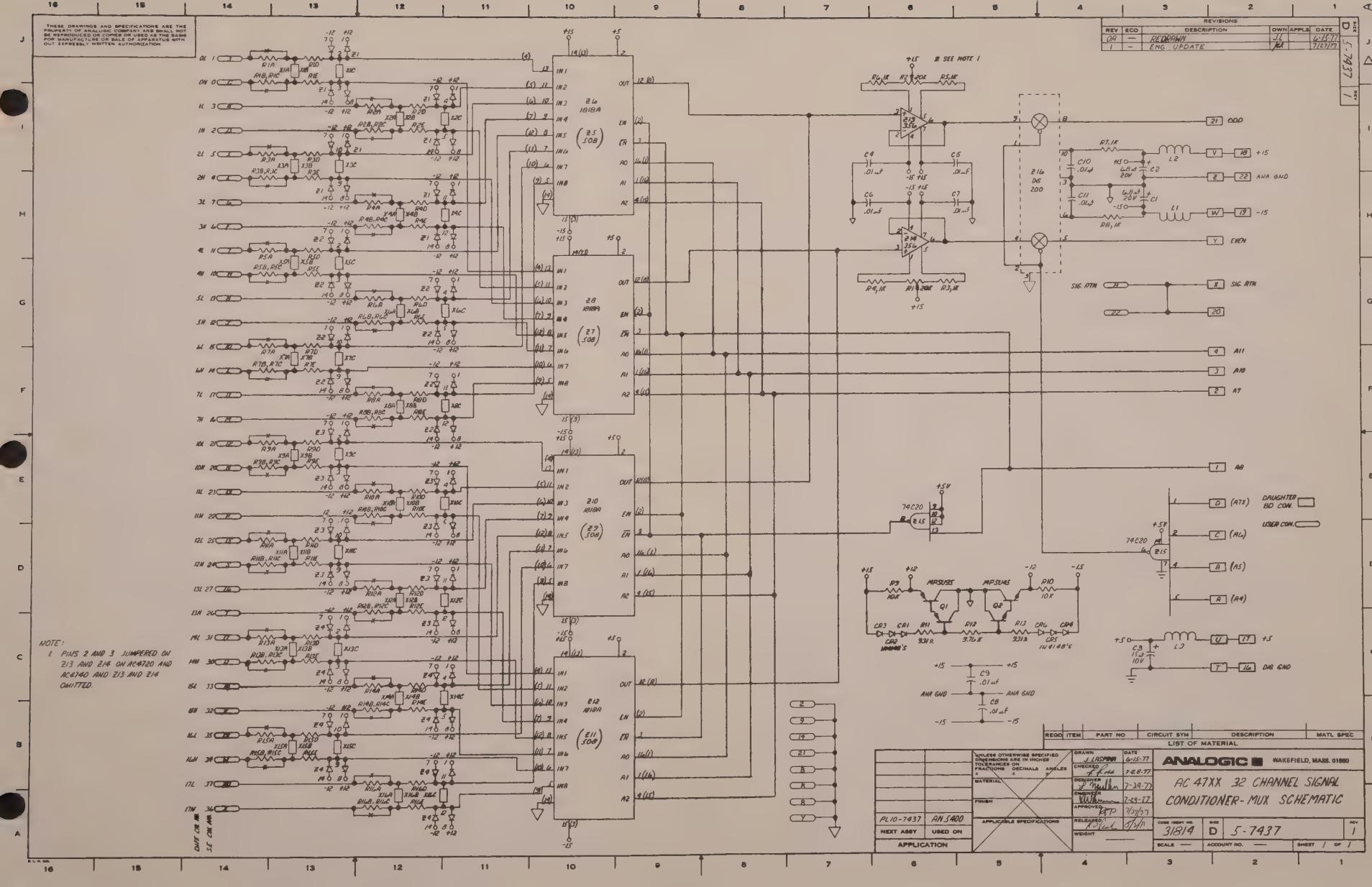
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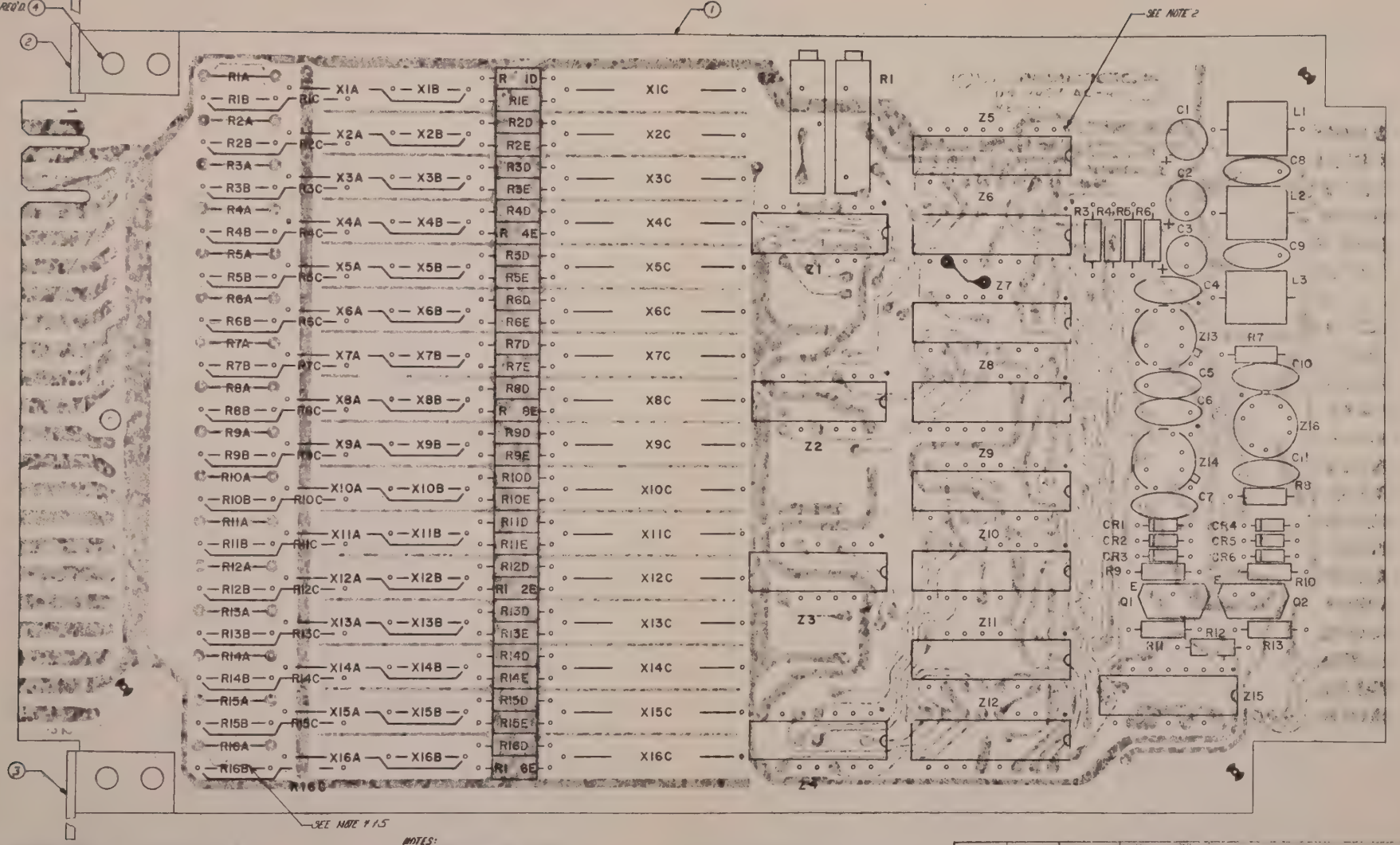
REVISIONS
REV ECO DESCRIPTION DWN APPR DATE
0A — RELEASED JC 6-15-77
1 — ENG. UPDATE 7/27/77
SIZE D 5-7437 REV 1
NOTE:
1. PINS 2 AND 3 JUMPERED ON Z13 AND Z14 ON AC4720 AND AC4740 AND Z13 AND Z14 OMITTED.
2 SEE NOTE 1
ODD
EVEN
ANA GND
SIG. RTN
DAUGHTER BD. CON.
USER CON.
DIG GND
+15
-15
+5
+5V
-12
-15
ANALOGIC WAKEFIELD, MASS. 01880
AC 47XX 32 CHANNEL SIGNAL CONDITIONER-MUX SCHEMATIC
CODE IDENT NO. 31814
SIZE D
5-7437
REV 1
SCALE —
ACCOUNT NO. —
SHEET 1 OF 1
LIST OF MATERIAL
REQD ITEM PART NO CIRCUIT SYM DESCRIPTION MATL SPEC
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN J. LASPINA 6-15-77
CHECKED J. KALL 7-28-77
DESIGNER 7-29-77
ENGINEER 7-29-77
APPROVED 7/29/77
RELEASED 8/1/77
WEIGHT
PL10-7437 AN 5400
NEXT ASSY USED ON
APPLICATION



REVISIONS						
REV	ECO	DESCRIPTION	DWN	APPR'D	DATE	
1	-	ENGINEERING UPDATE	JJ		7-21-77	D
						7-7437
						1

NOTES:
1. FOR SCHEMATIC SEE D5-7437.
2. DOT INDICATES PIN 1 OF I.C.'S.
3. ASSEMBLE IN ACCORDANCE WITH MC-1027.
4. CUT ETCH BETWEEN BRACKETS ON COMPONENT SIDE BEFORE INSTALLING RESISTORS FOR MODELS AC4730, 31, 32, 33.
5. CUT ETCH BETWEEN BRACKETS ON WIRING SIDE OF BOARD FOR MODELS AC4730, 31, 32, 33, 50, 51, 52, 53, 54.

COMPONENT SIDE

		J. USOPINA	7-21-77	ASSEMBLY AC 47XX 32 CHAN. SIG. CONDITIONER MUX
		L. Ross	7-28-77	
		L. Mullen	12-29-77	
			12-29-77	
			1/31/78	
PART NO. 7437	MC-47XX			SIZE 31814 D 7-7437 1
NEXT ASSY	USED ON			SCALE 4:1 DRAWING NO. SHEET 1 OF 1
APPLICATION				

11
D/A Converters

Card Number	Drawing Number	Title
AC1320/AC1330	—	AC1320/AC1330 Analog Output Modules Data Sheet
AC1320/AC1330	C5-7515	AC1320/AC1330 Dual Current Output DAC's Schematic
AC1320/AC1330	D7-7515	AC1320/AC1330 Dual Current Output DAC's Assembly
AC1520/AC1530	—	AC1520/AC1530 Analog Output Modules Data Sheet
AC1520/AC1530	D5-7514	AC1520/AC1530 Dual DAC Output Modules Schematic
AC15XX	D7-7514	AC15XX Dual DAC Output Module Assembly
AC1562	—	AC1562 Analog Output Modules Data Sheet
AC1562	C5-7424	AC1562 4 Channel, 12 Bit DAC Schematic
AC1562	D7-7424	AC1562 4 Channel, 12 Bit DAC Assembly
AC1700	D5-8673	AC1700 Isolated 4 Channel Bridge Balancing DAC Schematic
AC1700	D7-8673	AC1700 Isolated 4 Channel Bridge Balancing DAC Assembly
AC1813/AC1814	—	AC1813/AC1814 Analog Output Modules Data Sheet
MP1814	—	MP1814 14 Bit DAC Data Sheet
AC1813/AC1814	C5-7426	AC1813/AC1814 Dual DAC Output Module Schematic
AC1813/AC1814	D7-7426	AC1813/AC1814 Dual DAC Output Module Assembly
AC1900	—	AC1900 Series ADC Data Sheet
1900A	—	1900A Series 13, 14, 15, & 16 Bit DAC's Data Sheet
1900TC	—	1900TC Series 14, 15, & 16 Bit DAC's Data Sheet
AC1900XX	C5-7427	AC19XX, AC19XXTC, AC19XXRB, AC19XXTCRB Schematic
AC1913/AC1916	D7-7427	AC1913/AC1916 1 Channel, 13 & 14 Bit DAC's Assembly

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AC1320/AC1330

ANALOG OUTPUTS FOR AN5400

GENERAL

The AC1320/AC1330 are true current output analogs for the AN5400 Data Acquisition and Distribution System. The AC1320 card contains two complete 12 bit digital-to-analog converters including address and control logic, storage registers, precision voltage reference, and output amplifiers. The AC1330 contains two sixteen bit tri-state buffers allowing digital readback capability in addition to the circuitry of the AC1320.

Ordering Code:

Normally the two DACs on each board will be configured for the same output range. Two different ranges can be accommodated if specially ordered from the factory or if altered in the field.

AC13XX — X

1320 = 2 DACs
1330 = 2 DACs + Digital Readback

R = 0-20mA
S = 4-20mA
T = 0-50mA
U = 10-50mA

SPECIFICATIONS

Accuracy (@ 23°C):
Resolution: 12 Bits (Binary)
Relative Accuracy: ±0.012% FSR

Analog Output:
Available Full Scale Ranges:
0 — 20mA
4 — 20mA
0 — 50mA
10 — 50mA
Voltage Compliance: 12V or 24V with optional connection.
Load Capacitance: Unlimited

Speed:
Settling Time with 50Ω Load:
50usec. to 1/2 LSB

Stability:
Tempco of Range: ±15ppm/°C FSR Max.
Tempco of Offset: ±10ppm/°C FSR Max.
Tempco of Differential Linearity: ±3ppm/°C FSR Max.

Calibration Adjustments:
Full Scale Range: ±0.1% Min.
Offset: ±0.1% of FSR Min.

Digital Outputs:
CMOS Compatible
2 TTL Load Drive Capability

Digital Inputs:
10K Pullup to +5 on each input
Threshold: 1.5-3.5 Volts
CMOS — TTL Compatible

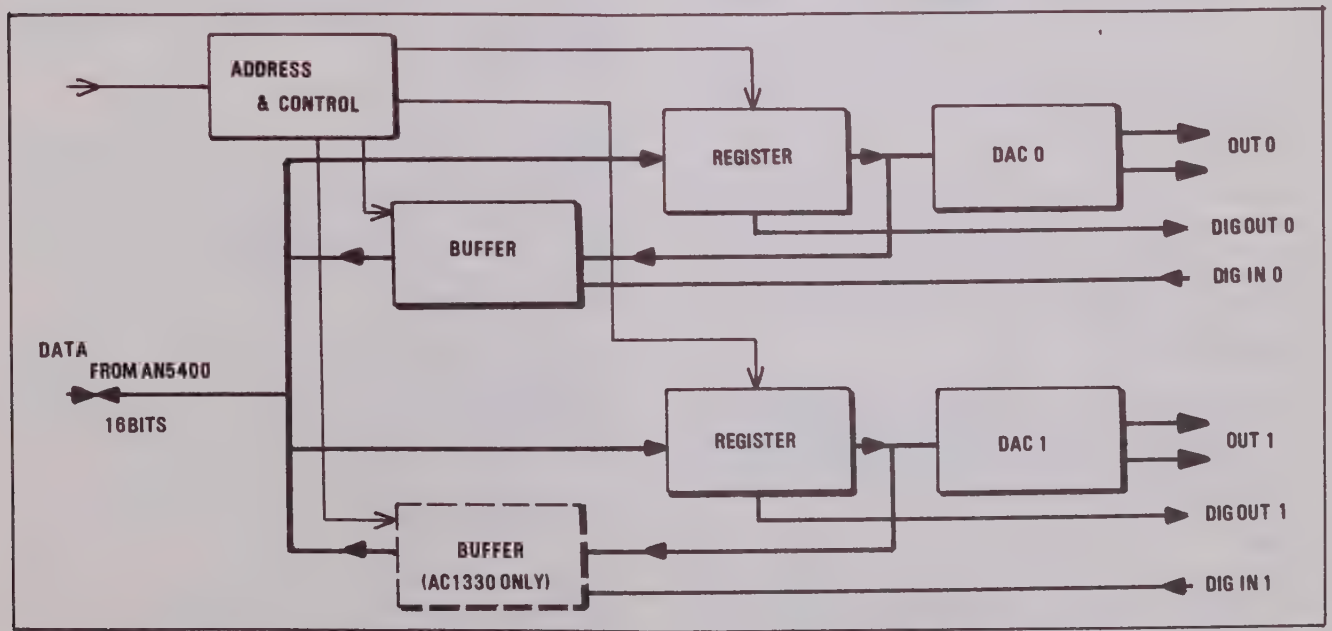

Figure 1. Block Diagram of AC1320

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. . . The Digitizers

LOAD CONNECTIONS

The AC1300 Series DACs are true current output DACs and include the excitation supply required in a current loop. Connections for a typical floating load are shown in Figure 2.

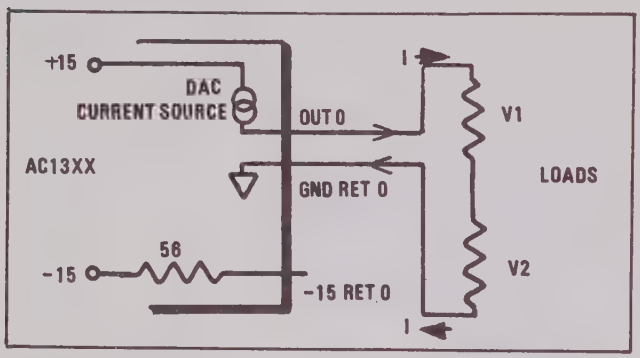


Figure 2. Connecting AC1300 to Floating Loads (Compliance≤ 12 volts)

The maximum compliance voltage between GND. Return and the Output is 12 Volts, thus the total load resistance must be less than 600Ω for 20mA full scale, or less than 240Ω for 50mA full scale. If the total load resistance exceeds these values, the -15 Return Line may be used to increase the compliance voltage, as shown in Figure 3.

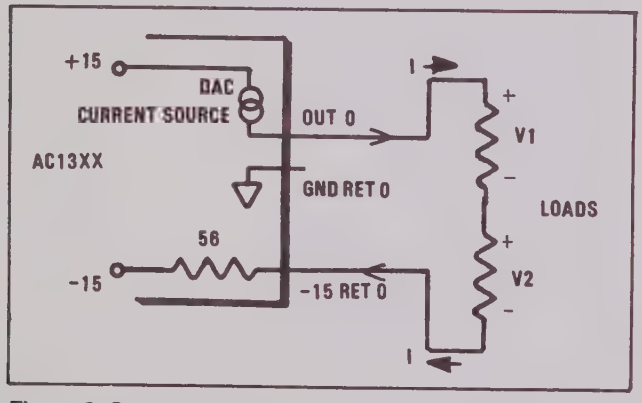


Figure 3. Connecting AC1300 to Floating Loads (Compliance ≤ 24 volts)

Now the compliance between -15 Return and the Output is 24 volts, allowing maximum load resistances of 1200Ω for 20mA full scale or 480Ω for 50mA full scale. **Accidental shorting of the -15 Return Line to GND. will cause minor component damage to the AC1300.**

DIGITAL OUTPUTS

The AC1320/1330 DACs are loaded with 16-bit parallel data in the normal manner described in Chapter 3 of the 5400 Manual and in the specification for the interface being used. The effect of this data on the card is shown below:

The four bits that are not used for the DAC are available at the user connector for any desired customer function.

DIGITAL INPUTS

The AC1330 only, when used in the Master Chassis of the AN5400, will supply digital inputs to the user's computer in the following format:

The four bits not supplied by the DAC register come from the user connector and can read any 5 Volt CMOS or TTL signal supplied by the customer.

The four digital outputs and four digital inputs available with each DAC are totally independent; but if it is desired to read back the digital outputs as digital inputs, note that the pins are conveniently placed across from one another and can be easily bussed together. In this manner complete equality between the 16 bit output word and the 16 bit input word is achieved.

CALIBRATION

Calibration of the AC1320/AC1330, when required, consists of adjusting the Offset and Range controls for each of the two DACs. These control potentiometers are located across the top edge of the P.C. card and can be accessed either by the use of an extender card (Analogic AC70) or by the removal of the AN5400 top cover. The relative location of the potentiometers is shown in Figure 3.

Calibration is most readily accomplished by measuring the voltage across a precision resistor to determine the current being supplied by the DAC. The accuracy of the calibration is determined by the DVM used (we suggest Data Precision Model 2540) and the accuracy to which the resistor value is known. Any resistor value may be used within the compliance constraints of the DAC.

After a 5-minute warmup, put the AN5400 into Local Control; Address DAC Ø on the card being calibrated; and apply the appropriate Data Inputs to the card as described in the Operating Instructions in Chapter 3 of the AN5400 Manual.

Apply the Data Code ØØØØØØ and adjust the Offset Control for the correct reading.

0-20mA : + 0.00mA (0.000V Across 100Ω)
4-20mA : + 4.00mA (0.400V Across 100Ω)
0-50mA : + 0.00mA (0.00V Across 100Ω)
10-50mA : +10.00mA (1.000V Across 100Ω)

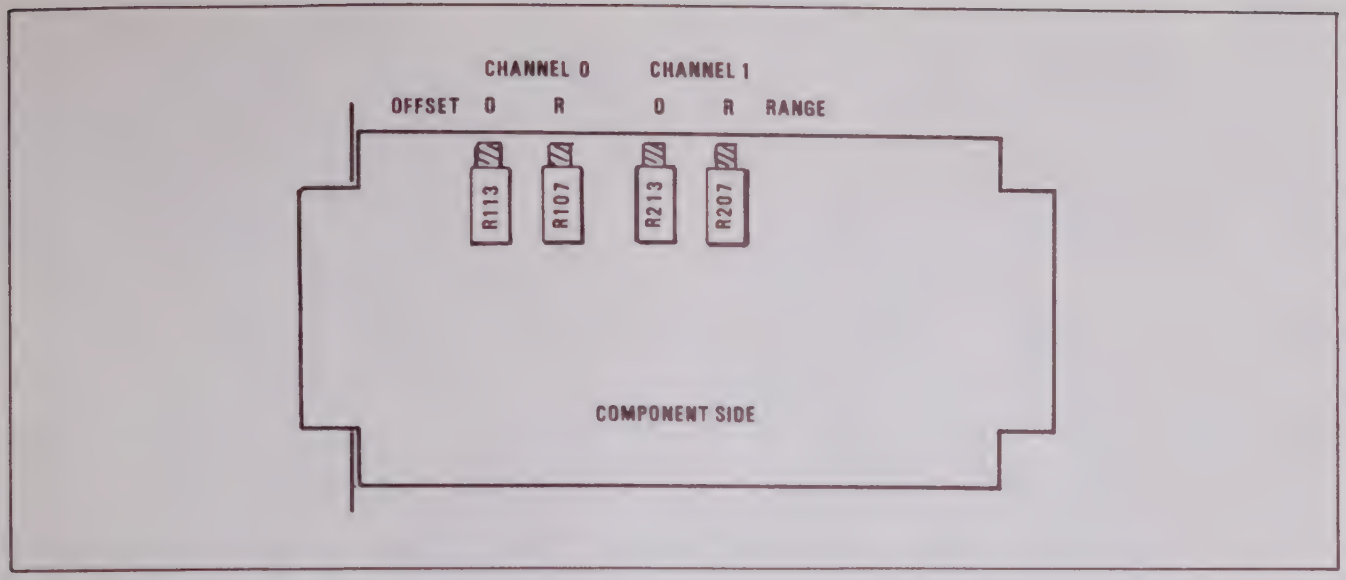


Figure 4. Location of Calibrating Adjustments

Apply the Data Code 177777 and adjust the Range Control for the correct reading.

0-20mA : +19.9951mA (1.99951V Across 100Ω)
4-20mA : +19.9960mA (1.99960V Across 100Ω)
0-50mA : +49.9878mA (4.99878V Across 100Ω)
10-50mA : +49.9902mA (4.99902V Across 100Ω)

Repeat the Offset and Range adjustments until no further adjustment is needed. When adjusting for 0.00mA, set the offset pot for a small positive reading and slowly back off just until 0.00mA is reached. Since the DAC is a unipolar device, further turning of the pot will not result in a negative current. Repeat adjustments for DAC 1.

PIN CONNECTIONS (USER)

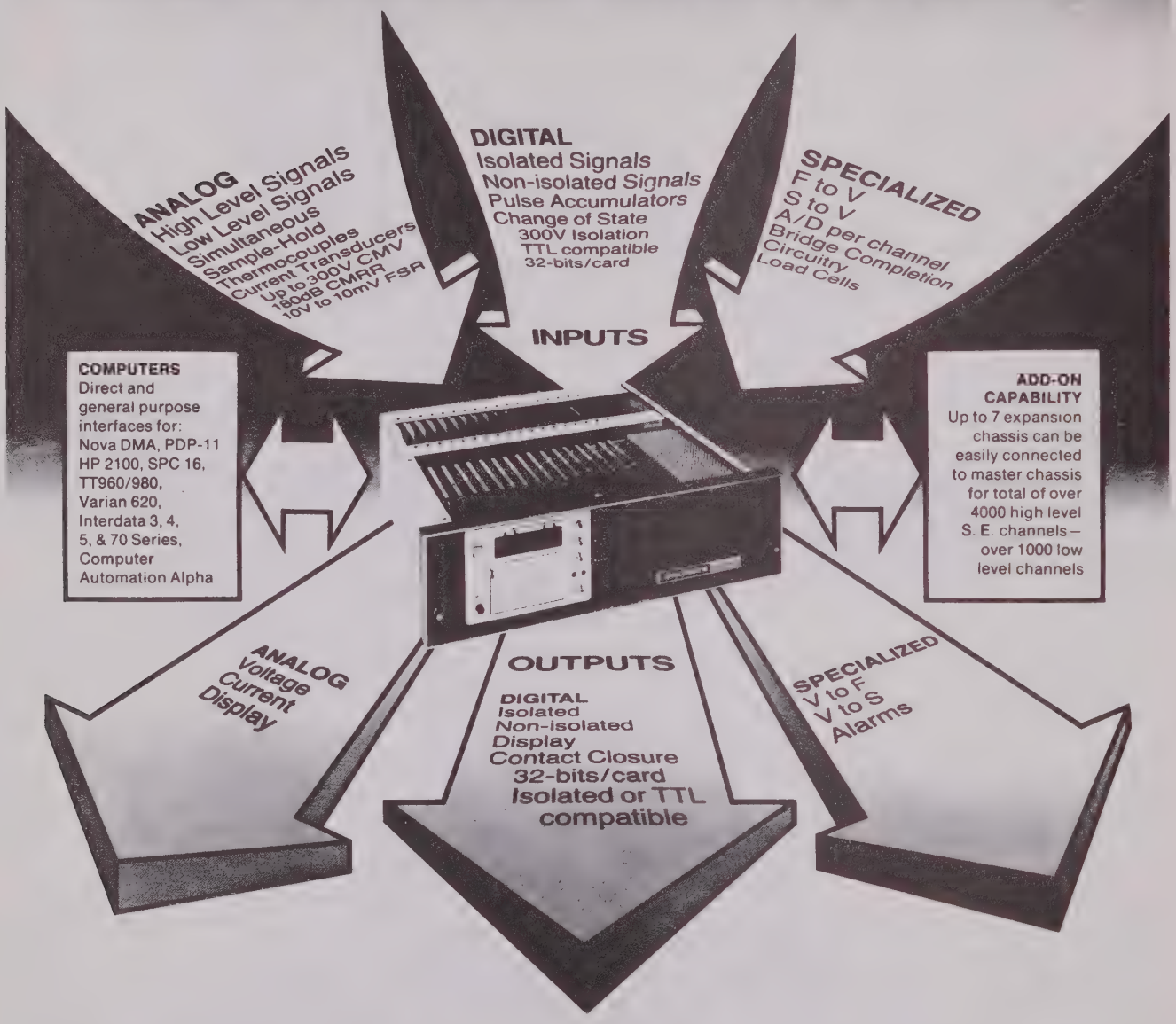
	Analog Ground	-A	1- Analog Ground
*	0 Input 16 (LSB)	-B	2- 0 Output 16 (LSB)
*	0 Input 15	-C	3- 0 Output 15
	DAC Output 0	-D	4
	GND. Return 0	-E	5- -15 Return 0
*	0 Input 14	-F	6- 0 Output 14
*	0 Input 13	-H	7- 0 Output 13
		J	8
		K	9
		L	10
		M	11
		N	12
	DAC Output 1	-P	13
	GND. Return 1	-R	14- -15 Return 1
*	1 Input 16 (LSB)	-S	15- 1 Output 16 (LSB)
*	1 Input 15	-T	16- 1 Output 15
		U	17
		V	18
*	1 Input 14	-W	19- 1 Output 14
*	1 Input 13	-X	20- 1 Output 13
	Digital Ground	-Y	21- Digital Ground
	Analog Ground	-Z	22- Analog Ground

* AC1330 Only

SYSTEM ENGINEERS...

put yourself in control

WITH ANALOGIC'S AN5400 BUILDING BLOCK DATA ACQUISITION SYSTEM



The AN5400 Installation...

is usually the simplest and most troublefree part of the assembly and proving out of any large system. There are many reasons for this, but chief among them are exhaustive pre-shipment computer-programmed testing to verify specified performance; complete access to all signal and control input/output cabling and input/output modules; generous performance margins in all module designs; and the "stand-alone", self-powered nature of the AN5400.

The Analogic Customer...

has available to him the extensive resources of Analogic's Applications and Field Engineering staffs, including regional Field Managers with direct access to the factory backup. We are always ready to consult on new requirements, upgrading and expansion of existing systems, and major system reconfiguration.

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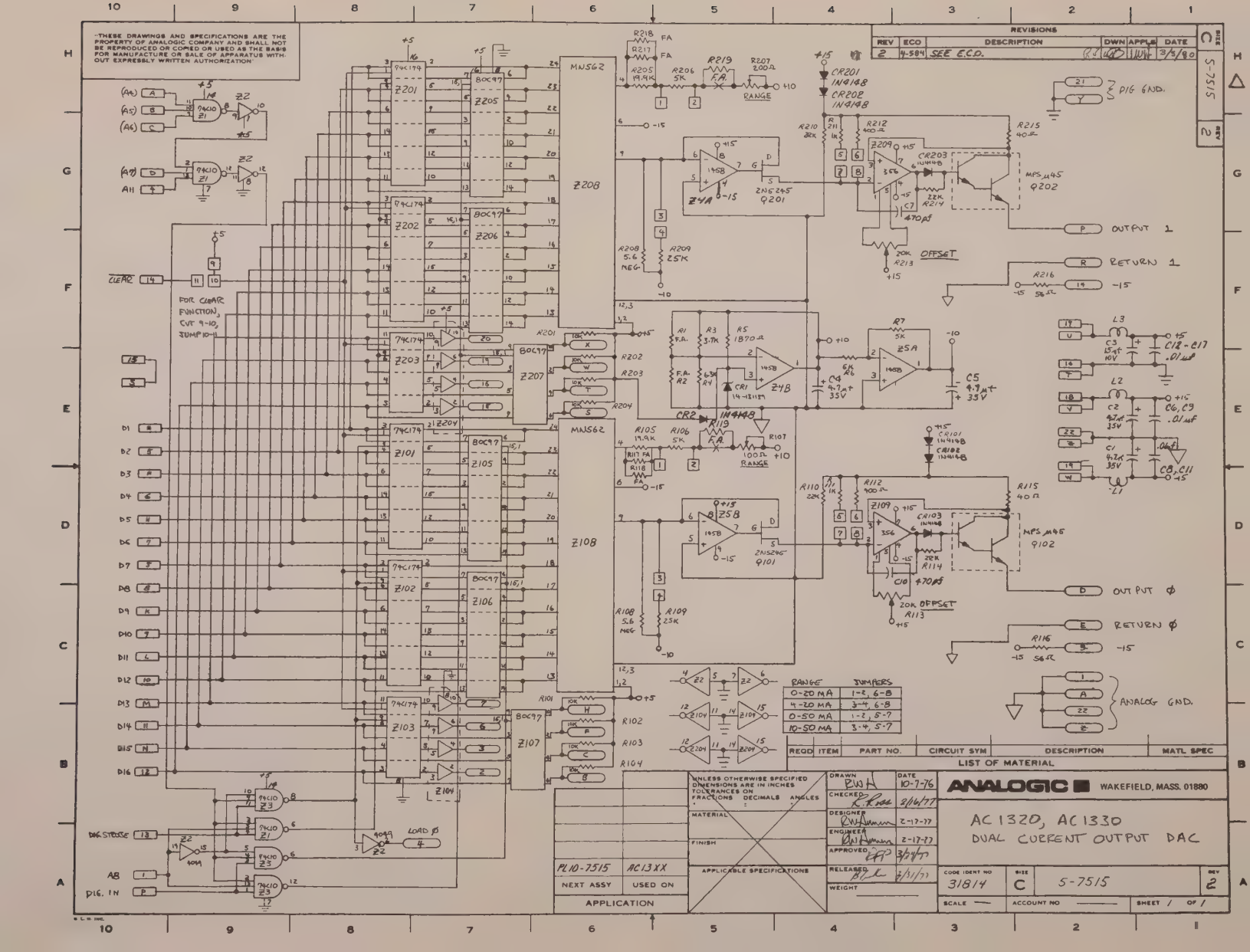
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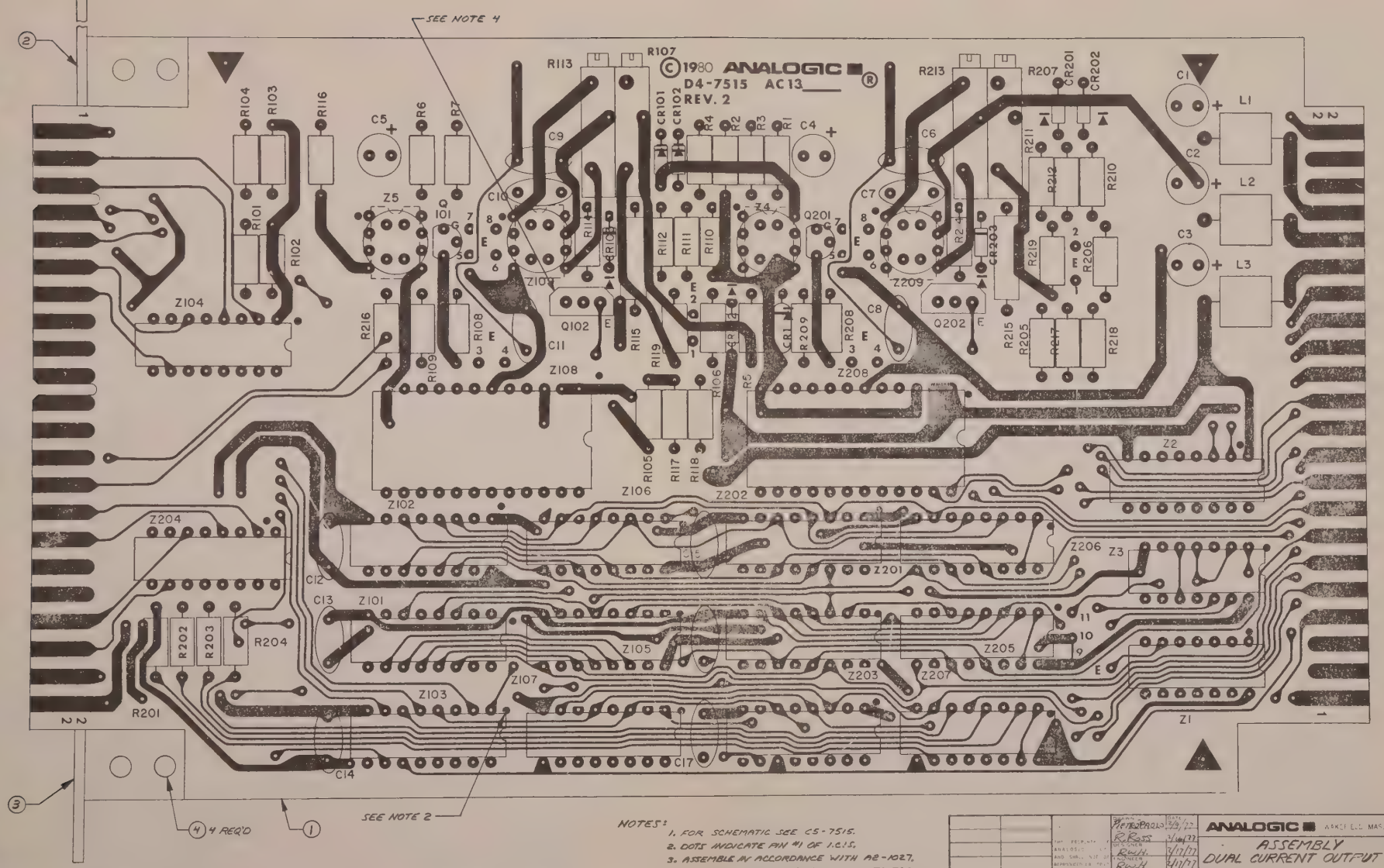
REVISIONS
REV ECO DESCRIPTION DWN APPD DATE
2 4-584 SEE E.C.O. RWH 3/5/80
SIZE C 5-7515 REV 2
FOR CLEAR FUNCTION, CUT 9-10, JUMP 10-11
RANGE JUMPERS
0-20 MA 1-2, 6-8
4-20 MA 3-4, 6-8
0-50 MA 1-2, 5-7
10-50 MA 3-4, 5-7
REQD ITEM PART NO. CIRCUIT SYM DESCRIPTION MATL SPEC
LIST OF MATERIAL
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN RWH 10-7-76
CHECKED K. Ross 2/16/77
DESIGNER RWH 2-17-77
ENGINEER RWH 2-17-77
APPROVED 3/7/77
RELEASED 3/31/77
WEIGHT
PL10-7515 AC13XX
NEXT ASSY USED ON
APPLICATION
ANALOGIC WAKEFIELD, MASS. 01880
AC1320, AC1330
DUAL CURRENT OUTPUT DAC
CODE IDENT NO 31814
SIZE C 5-7515 REV 2
SCALE
ACCOUNT NO
SHEET / OF /
CLEAR
DIG STROBE
AB
DIG. IN
LOAD Ø
DIG GND.
OUTPUT 1
RETURN 1
OUTPUT Ø
RETURN Ø
ANALOG GND.
OFFSET
RANGE
MPS U45 Q202
MPS U45 Q102
2N5245 Q201
2N5245 Q101
MUX62
BOC97
74C174



NOTES:

1. FOR SCHEMATIC SEE C5-7515.
2. DOTS INDICATE PIN #1 OF I.C.'S.
3. ASSEMBLE IN ACCORDANCE WITH A2-1027.
4. CUT TABS ON Q102 & Q202 FLUSH TO BODY.
5. MAX. COMP. HEIGT .500.

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPR'D	DATE
2	4-384	SEE ECO.	RJB	RWK	3-10-80

DRAWN	R.ROSS	3/9/77	ANALOGIC	ANALOG DEVICES, INC. MASS. 01880
DATA CHECK	R.ROSS	3/16/77	ASSEMBLY	
ANALOGIC ENGINEER	RWK	3/17/77	DUAL CURRENT OUTPUT DAC	
APPROVED	RWK	4/1/77	AC1320, 1330	
QUALITY ASSURANCE	RFB	3/18/77		
M. MFG.	R. PEAK	3/24/77	31814	D 7-7515 2
PL10-7515 AC13XX				
NEXT ASSY	USED ON			
APPLICATION			SCALE 4:1	SHEET 1 OF 1

AC1520/AC1530

ANALOG OUTPUT FOR AN54000

GENERAL DESCRIPTION

The AC1520 is an analog output card for the AN5400 Data Acquisition System. This card contains two complete 12-bit digital to analog converters, including address and control logic, storage registers, precision voltage reference, and output amplifiers. In addition, it features two 4-bit digital output ports.

The AC1530 contains all of the above plus two 16-bit tristate buffers, allowing readback of each DAC register, and two four-bit digital input ports. System inputs, power requirements, mechanical dimensions compatible with AN5400.

SPECIFICATIONS

ACCURACY (@23°C):
Resolution: 12 bits (binary)
Relative accuracy: ±.012% FSR

ANALOG OUTPUT:
Full scale ranges: ±10V, ±10.24V
±5V, ±5.12V
0–10V, 0–10.24V
0–5V, 0–5.12V
Impedance: less than 0.1 ohm D.C.
Load Current: ±10mA
Short circuit duration: unlimited
Load capacitance: 5000 pf
Ground sense compensation: ±1V

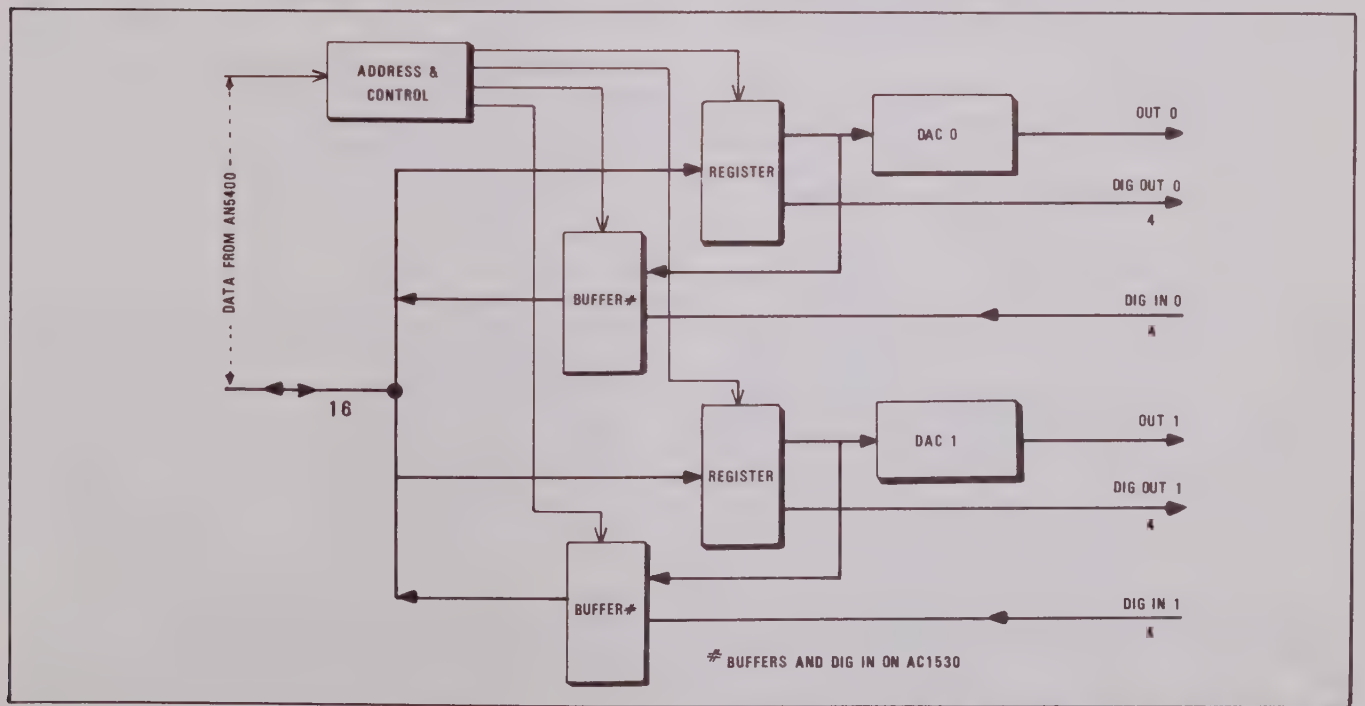
SPEED: (1000pf load)
Settling time to 1/2LSB: 10μsec
Slew rate: 10V/μsec typ.

STABILITY: (Tempco)
Range: ±15 ppm/°C FSR max.
Offset: ±10 ppm/°C FSR max.
Differential Linearity:
±3 ppm/°C FSR max.

CALIBRATION ADJUSTMENTS:
Full scale range: ±0.1% min.
Offset: ±0.1% of FSR min.

DIGITAL OUTPUTS:
CMOS compatible
2 TTL load drive capability

DIGITAL INPUTS:
10K pullup to +5V on each input.
Threshold: 1.5–3.5 volts
CMOS — TTL compatible



AC1520/AC1530 BLOCK DIAGRAM

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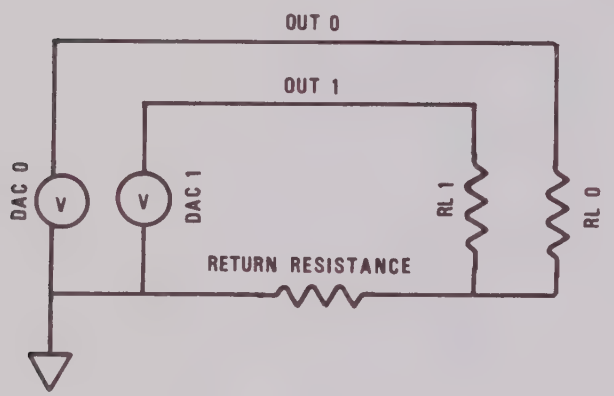
. . . The Digitizers

LOAD CONNECTIONS

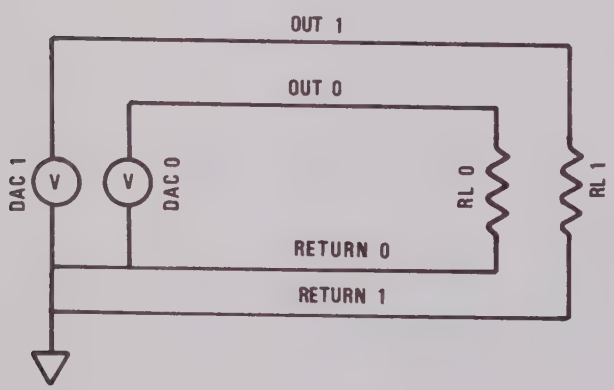
The AC1530, AC1520 provides separate return and return sense lines for each DAC output, thus maintaining full accuracy at the load terminals. Proper usage of the return and return sense lines will eliminate most ground loop problems.

FLOATING LOADS

When driving true floating loads it is not necessary to use the return sense lines, but they must be tied to their respective returns at the DAC card connector. However, it is important to use the separate return lines for each DAC. Consider the following example:



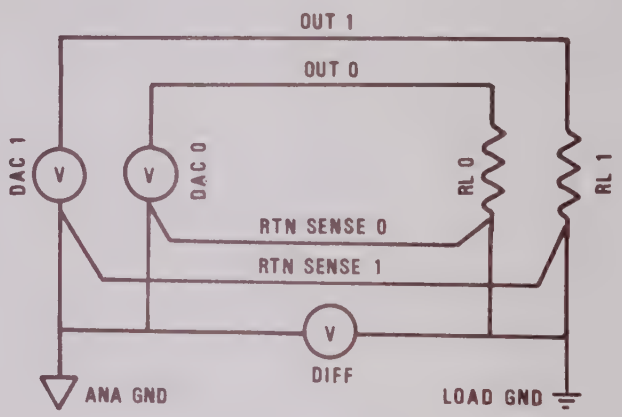
Notice that the voltage across RL1 will be changed if the output of DAC 0 changes, because of the common return lead resistance shared by the two loads. The correct way to connect floating loads is as follows:



This use of separate return lines avoids crosstalk between DACs.

GROUNDED LOADS

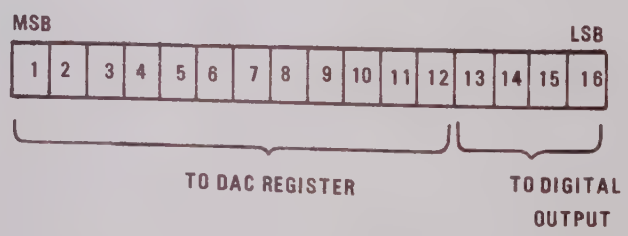
Often the loads to be driven by the DACs will not be floating, but will be grounded to other items, e.g., power supply returns, chassis grounds, AC power grounds, etc. In complex grounding schemes an unavoidable potential difference may exist between the AN5400 analog ground and the low side of the load. To alleviate this problem the AC1530/1520 has return sense leads that function in a manner similar to power supply remote sense leads.



Connection of the return sense lead directly to the low side of the load will cause each DAC to compensate for voltage difference between grounds, up to ±1 volt.

DIGITAL OUTPUTS

The AC1530, 1520 DACs are loaded with 16 bit parallel data in the normal manner described in Chapter 3 of the 5400 Manual and in the specification for the interface being used. The effect of this data on the card is shown below.



The four bits that are not used for the DAC are available at the user connector for any desired customer function.

DIGITAL INPUTS

The AC1530 only, when used in the Master Chassis of the AN5400, will supply digital inputs to the user's computer in the following format:

The four bits not supplied by the DAC register come from the user connector and can read any 5 volt CMOS or TTL signal supplied by the customer.

The four digital outputs and four digital inputs available with each DAC are totally independent; but if it is desired to read back the digital outputs as digital inputs, note that the pins are conveniently placed across from one another and can be easily bussed together. In this manner complete equality between the 16 bit output word and the 16 bit input word is achieved.

LOAD 0 OUTPUT

A positive pulse is supplied to the user that occurs immediately prior to updating of digital and DAC data on channel 0. This pulse is available to generate a blanking signal, control deglitching circuitry, or initiate any other customer required function.

CALIBRATION INSTRUCTIONS

Calibration of the AC1530, AC1520 consists of adjusting the offset and range controls for each DAC. These control potentiometers are located across the top edge of the PC card and can be accessed by removing the AN5400 top cover or by removing the AC1530 and placing it on an extender card (Analogic AC70). Control locations are shown below:

Connect a precision, high impedance DVM (e.g. Data Precision Model 2540) between the output and return sense pins of each DAC as it is calibrated. Allow a 5 minute warm-up.

ZERO CALIBRATION

Put the AN5400 into local control. Address DAC 0 on the card being calibrated, and apply the appropriate data inputs to the card as described in the operating instructions in Chapter 3 of the AN5400 manual. Apply the data input that will give the **lowest** output voltage from the DAC. For a binary DAC this will be octal code 000000. For a two's complement DAC, this will be an octal 100000. Adjust the offset potentiometer for the correct DVM reading according to the chart below.

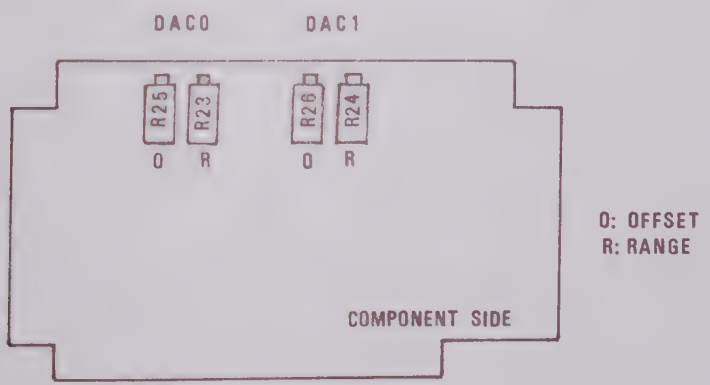
0 to 10V	= 0.0000	±10.24V	= −10.2400
±10V	= −10.0000	0 to 10.24V	= 0.0000
± 5V	= −5.0000	±5.12V	= −5.1200
0 to 5V	= 0.0000	0 to 5.12V	= 0.0000

RANGE CALIBRATION

To perform the range adjustment, apply the data code that results in the most positive DAC output voltage. For a binary DAC, this will be an octal code of 177777. For a two's complement DAC, this will be an octal code of 077777. Adjust the range potentiometer for the correct range reading according to the chart below.

0 to 10V	= +9.9976	±10.24V	= +10.2350
±10V	= 9.9951	0 to 10.24V	= +10.2375
± 5V	= +4.9976	± 5.12V	= +5.1175
0 to 5V	= +4.9988	0 to 5V	= +5.1187

Because of a slight interaction, repeat the Offset and Range adjustments until no further adjustment is required. After moving the DVM leads to the next DAC output, perform the Offset and Range adjustment procedure until each DAC has been calibrated.



ORDERING CODE:

Normally, both DACs will be configured for the same voltage range. Coding is shown below:

To Order	AC 15□-□
2 DACs & digital outputs	20
2 DACs & digital outputs & digital inputs & readback	30
Full Scale Range	
0–10V Binary	1A
±10V 2's Comp.	2D
±5V 2's Comp.	3D
0–5V Binary	4A
±10.24V 2's Comp.	5D
0–10.24V Binary	6A
±5.12V 2's Comp.	7D
0–5.12V Binary	8A

On special request, the two DACs may be configured differently within the groups 1A to 4A, or 5D to 8A. Combinations such as 0–10V and 0–10.24V are not allowed however.

Pin Connections (User)

Analog gnd.	A	1	Analog gnd.
0 input 16 (LSB)	B	2	0 output 16 (LSB)
0 input 15	C	3	0 output 15
0 DAC output	D	4	0 DAC load output
0 DAC gnd. rtn.	E	5	0 DAC rtn. sense
0 input 14	F	6	0 output 14
0 input 13	H	7	0 output 13
	J	8	
	K	9	
	L	10	
	M	11	
	N	12	
1 DAC output	P	13	
1 DAC gnd. rtn.	R	14	1 DAC rtn. sense
1 input 16 (LSB)	S	15	1 output 16 (LSB)
1 input 15	T	16	1 output 15
	U	17	
	V	18	
1 input 14	W	19	1 output 14
1 input 13	X	20	1 output 13
Digital Gnd.	Y	21	Digital Gnd.
Analog Gnd.	Z	22	Analog Gnd.

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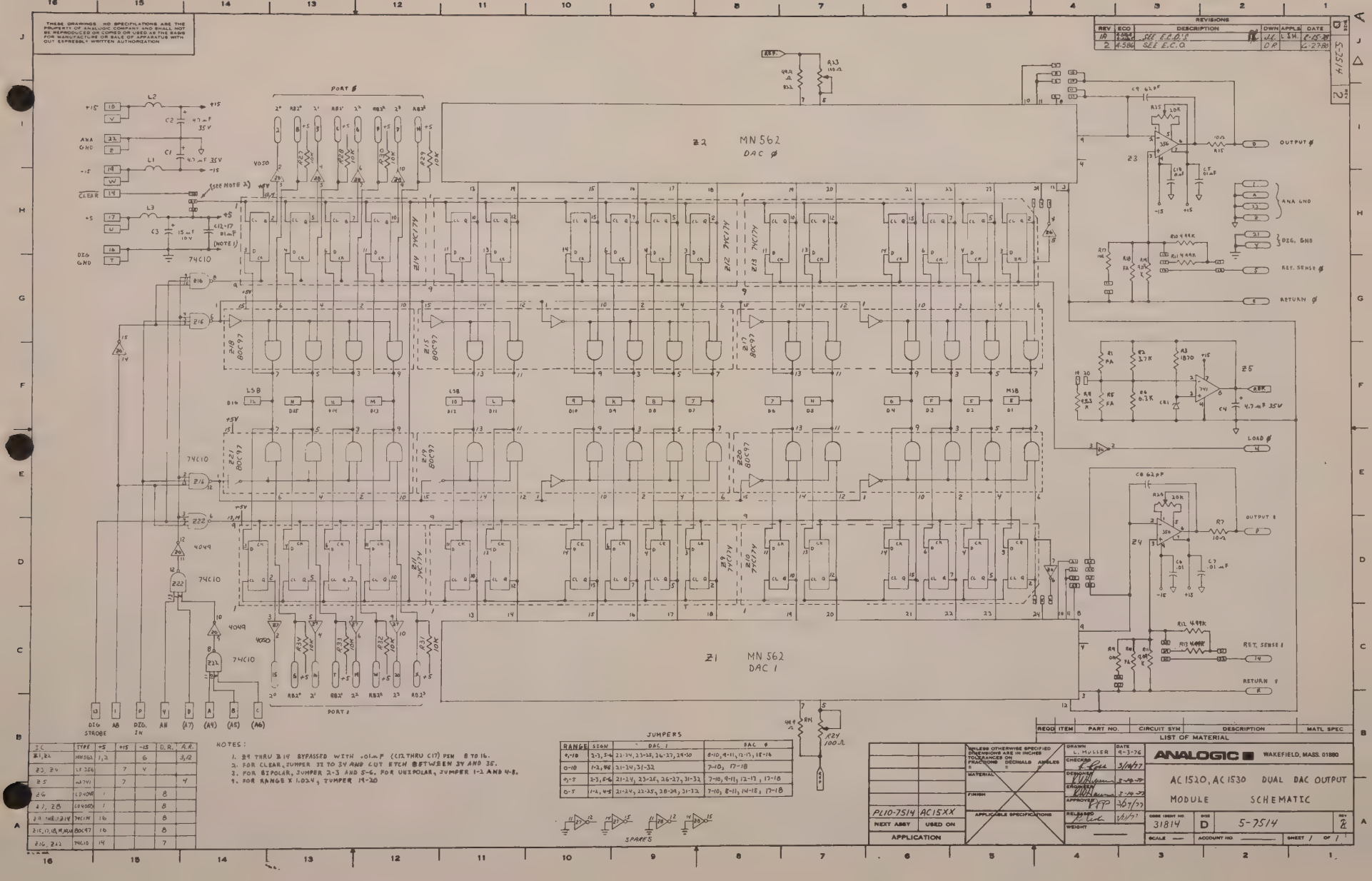
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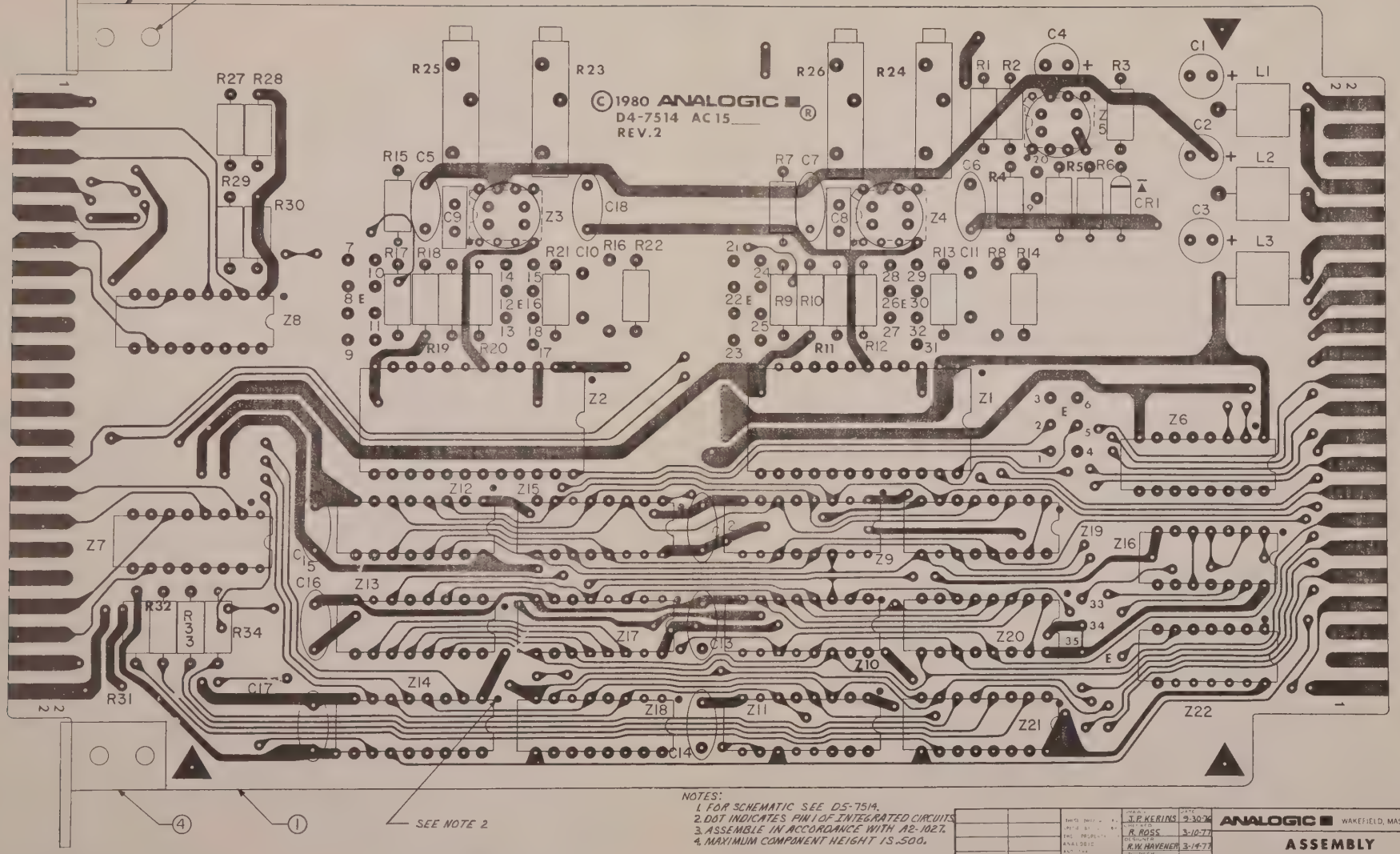
REVISIONS
REV ECO DESCRIPTION DWN APPR DATE
1D 4-5867 SEE E.C.O.'S JL L.M. 6-15-77
2 4-5867 SEE E.C.O. DP 6-27-77
4-1513
Z2 MN562 DAC 0
Z1 MN562 DAC 1
PORT 0
PORT 1
74C10
4049
4050
ALS74
BDC97
OUTPUT 0
OUTPUT 1
RET. SENSE 0
RET. SENSE 1
RETURN 0
RETURN 1
ANA GND
DIG. GND
LOAD 0
DIG STROBE
DIG. IN
JUMPERS
RANGE SIGN DAC 1 DAC 0
0-10 2-3, 5-6 21-24, 23-25, 26-27, 28-30 8-10, 9-11, 12-13, 14-16
0-10 1-2, 4-5 21-24, 31-32 7-10, 9-11, 12-13, 17-18
0-5 2-3, 5-6 21-24, 26-27, 31-32 7-10, 9-11, 12-13, 17-18
0-5 1-2, 4-5 21-24, 23-25, 28-29, 31-32 7-10, 8-11, 14-15, 17-18
2 SPARES
NOTES:
1. 2# THRU 2#19 BYPASSED WITH .01uF (C12 THRU C17) PIN 8 TO 16.
2. FOR CLEAR, JUMPER 32 TO 34 AND CUT ETCH BETWEEN 34 AND 35.
3. FOR BIPOLAR, JUMPER 2-3 AND 5-6. FOR UNIPOLAR, JUMPER 1-2 AND 4-5.
4. FOR RANGE X 1.024, JUMPER 19-20
IC TYPE +5 +15 -15 D.R. A.R.
Z1, Z2 MN562 1,2 6 3,4
Z3, Z4 LF 356 7 4
Z5 μA741 7 4
Z6 CD4049 1 8
Z7, Z8 CD4050 1 8
Z9 THRU Z14 74C174 16 8
Z15, 17, 18, 19, 20, 24 BDC97 16 8
Z16, Z23 74C10 14 7
REQD ITEM PART NO. CIRCUIT SYM DESCRIPTION MATL SPEC
LIST OF MATERIAL
PL10-7514 AC15XX
NEXT ASSY USED ON
APPLICATION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
WEIGHT
DRAWN L. MUELLER DATE 4-3-76
CHECKED 3/14/77
DESIGNED
ENGINEER
APPROVED 3/7/77
RELEASED 4/1/77
ANALOGIC WAKEFIELD, MASS. 01880
AC1520, AC1530 DUAL DAC OUTPUT MODULE SCHEMATIC
CODE IDENT NO. 31814
SIZE D
5-7514
REV Z
SCALE
ACCOUNT NO.
SHEET 1 OF 1



NOTES:
1. FOR SCHEMATIC SEE D5-7514.
2. DOT INDICATES PIN 1 OF INTEGRATED CIRCUITS.
3. ASSEMBLE IN ACCORDANCE WITH A2-1027.
4. MAXIMUM COMPONENT HEIGHT IS .500.

COMPONENT SIDE

REVISIONS					
REV.	ECO	DESCRIPTION	DWN	APPD'S	DATE
2	1586	SEE E.C.O.	D.R.		6-21-80

		J.P. KERINS	9-30-76
		R. ROSS	3-10-77
		R.W. HAVENER	3-14-77
		R.W. HAVENER	3-14-77
		R.F. POWELL	3-29-77
		R. PEAKE	3-31-77
PL10-7514 AC15 xx			
NEXT ASSY	USED ON		
APPLICATION			

ANALOGIC WAKEFIELD, MASS 01880

ASSEMBLY
DUAL DAC OUTPUT
AC15___

CODE IDENT NO	SIZE		REV
31814	D	7-7514	2
SCALE 4:1	ACCOUNT NO		SHEET 1 OF 1

AC1562

ANALOG OUTPUT FOR ANDS5400

GENERAL DESCRIPTION

The AC1562 is an analog output card for the ANDS5400 Data Acquisition System. This card contains four complete 12-bit Digital to Analog converters, including address and control logic, storage registers, precision voltage reference, and output amplifiers. A simplified block diagram of this PC card is shown in Fig. 1. User pin assignments are identified in Table 1.

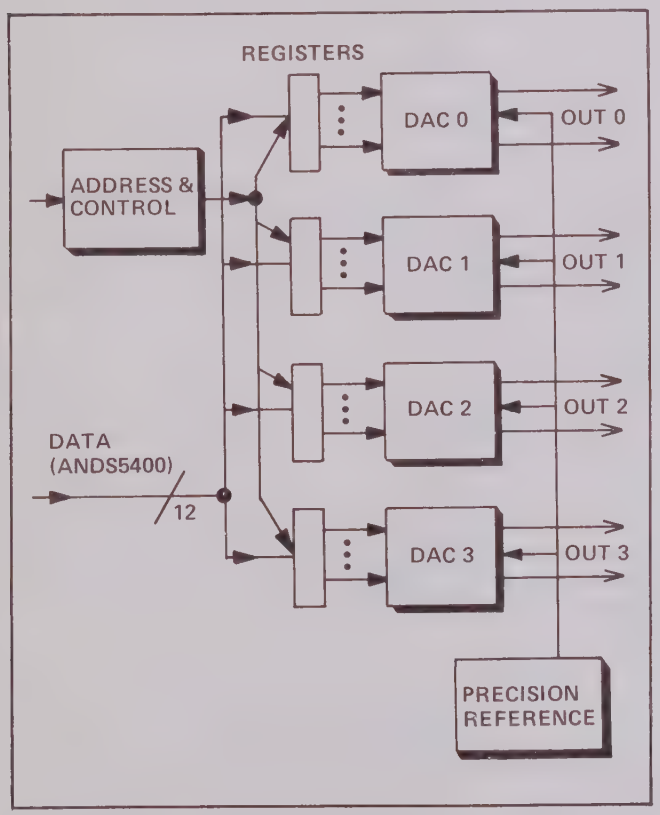


Fig. 1. AC1562 simplified block diagram.

APPLICATION DATA

Load Connections

The AC1562 provides separate return lines and separate return sense lines for each DAC output, thus maintaining full accuracy at the load terminals. Proper use of the return and return sense lines will eliminate most ground loop problems.

Floating Loads

When driving true floating loads it is not necessary to use the return sense lines; they can be left open or tied to their respective returns at the DAC card connector. However, it is important to use the separate return lines for each DAC, as shown in Fig. 2. The use of separate return lines avoids crosstalk between DACs.

SPECIFICATIONS

ACCURACY (@ 23°C)

Resolution: 12 bits (Binary) ± 1.19 mV
Relative Accuracy: ±0.012% FSR
Noise (10Hz – 100kHz): <0.01% FSR RMS

ANALOG OUTPUT

Available Full Scale Ranges
±10 V, ±10.24 V
±5 V, ±5.12 V
0-10 V, 0-10.24 V
0-5 V, 0-5.12 V

Impedance: less than 0.1 Ω DC
Load Current: ±10 mA
Short Circuit Duration: Unlimited
Load Capacitance: 5000 pF
Ground Sense Compensation: ±1 V

SPEED

Settling Time to ½ LSB: 10 μsec max. (with 1000 pF Load)
Slew Rate: 10 V/μsec typ (with 1000 pF Load)

STABILITY

Tempco of Range: ±15 ppm/°C FSR max
Tempco of Offset: ±10 ppm/°C FSR max
Tempco of Differential Linearity: ±3 ppm/°C FSR max

CALIBRATION ADJUSTMENTS

Full Scale Range: ±0.1%
Offset: ±10 mV

DIGITAL OUTPUT (LOAD 0 PULSE)

Drive Capability: 2 TTL Loads
Width: 200 nsec min, positive-going.

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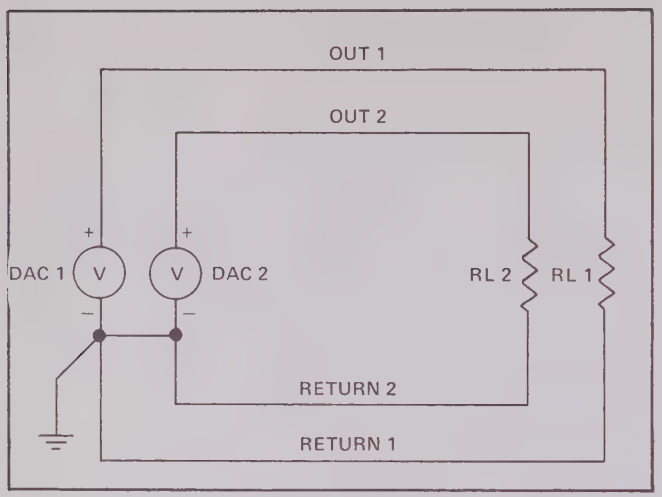

Fig. 2. Connections for floating loads.

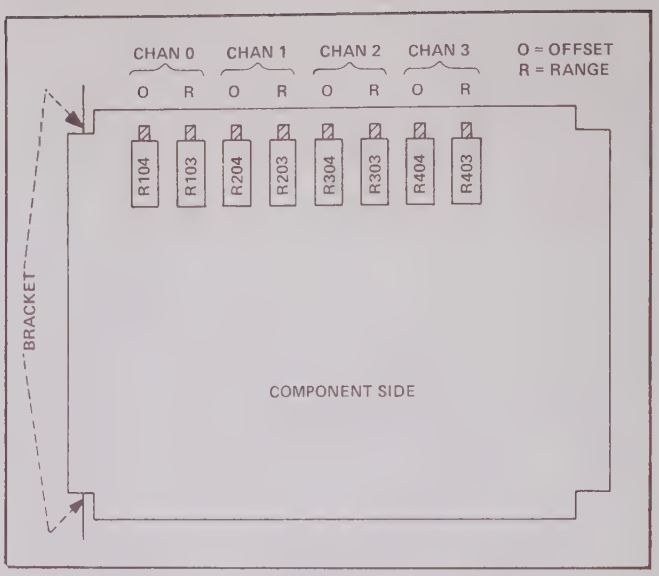

Fig. 3. Relative locations of adjustment controls.

APPLICATION DATA

Grounded Loads

Often the loads to be driven by the DACs will not be floating, but will be grounded to other items, e.g., power supply returns, chassis grounds, AC power grounds, etc. In complex grounding schemes an unavoidable potential difference may exist between the ANDS5400 analog ground and the low side of the load. To alleviate this problem, the AC1562 has return sense leads that function in a manner similar to power supply remote sense leads.

Connection of the return sense lead directly to the low side of the load will cause each DAC to compensate for voltage difference between grounds, up to ±1 volt.

LOAD 0 PULSE

A single digital output is provided from the DAC card. The Load 0 Pulse is a positive pulse that occurs immediately prior to the updating of DAC 0. This pulse is available to generate a blanking signal, control de-glitching circuitry, or initiate any customer required function. This signal can drive two TTL Loads and should be referenced to digital ground.

CALIBRATION INSTRUCTIONS

Calibration of the AC1562, when required, consists of adjusting the Offset and Range controls for each of the four DACs. These control potentiometers are located across the top edge of the PC card and can be accessed either by the use of an extender card (AC70) or by removal of the ANDS5400 top cover. The relative location of the potentiometers is shown in Fig. 3. Connect a precision, high impedance DVM (e.g.: Data Precision Model 2540) between the Output and the Return Sense pins of each DAC as it is calibrated. Refer to pin connections in Table 1. After a 5-minute warmup, calibrate Channel Zero as follows:

Put the ANDS5400 into Local control; address DAC 0 on the card being calibrated; apply the appropriate data inputs to the card as described in the operating instructions in Chapter 3 of the ANDS5400 manual. Apply the data input that will give the lowest voltage output from the DAC. For a binary DAC, this will be an octal code of 000000. For a two's complement DAC, this will be an octal code of 100000. Adjust the Offset potentiometer for the correct DVM reading according to the chart.

0 to 10 V =	0.0000	±10.24 V =	−10.2400
±10 V =	−10.0000	0 to 10.24 V =	0.0000
± 5 V =	−5.0000	±5.12 V =	−5.1200
0 to 5 V =	0.0000	0 to 5.12 V =	0.0000

To perform the Range adjustment, apply the data code that results in the most positive DAC output voltage. For a binary DAC, this will be an octal code of 177777. For a two's complement DAC, this will be an octal code of 077777. Adjust the Range potentiometer for the correct range reading according to the chart below.

0 to 10 V =	+9.9976	±10.24 V =	+10.2350
±10 V =	+9.9951	0 to 10.24 V =	+10.2375
± 5 V =	+4.9976	±5.12 V =	+5.1175
0 to 5 V =	+4.9988	0 to 5 V =	+5.1187

Repeat the Offset and Range adjustments until no further adjustment is required. After moving the DVM leads to the next DAC output, address the next DAC, perform the Offset and Range adjustment procedure until all four DACs have been calibrated.

Table 1
AC1562 User Pin Connections*

Analog Gnd	A	1	Analog Gnd
Out 0	D	4	Load 0
Return 0	E	5	Return Sense 0
Out 1	J	8	**
Return 1	K	9	Return Sense 1
Out 2	P	13	**
Return 2	R	14	Return Sense 2
Out 3	U	17	**
Return 3	V	18	Return Sense 3
Digital Gnd	Y	21	Digital Gnd
Analog Gnd	Z	22	Analog Gnd

*Unlisted pin terminals are not used.

**Not used

ADDRESSING

The address structure of the ANDS5400 provides complete flexibility of configuration and installation. Table 2 details the addresses of devices installed in any enclosure. To determine the absolute address of this device, simply add to the address indicated below the enclosure address in the Digital Output Mode (see ANDS5400 Manual).

Table 2
Address Locations (Octal)

J1	0, 1, 2, 3	J9	40, 41, 42, 43
J2	4, 5, 6, 7	J10	44, 45, 46, 47
J3	10, 11, 12, 13	J11	50, 51, 52, 53
J4	14, 15, 16, 17	J12	54, 55, 56, 57
J5	20, 21, 22, 23	J13	60, 61, 62, 63
J6	24, 25, 26, 27	J14	64, 65, 66, 67
J7	30, 31, 32, 33	J15	70, 71, 72, 73
J8	34, 35, 36, 37	J16	74, 75, 76, 77

Table 3
Full Scale Jumper Configurations

1A	0-10 V	B-D, C-E, F-H, K-M	Binary	E1-E3
2D	±10 V	A-D, N-P	2's Complement	E2-E3
3D	±5 V	A-D, C-E, F-H, N-P		
4A	0-5 V	A-D, B-E, J-K, N-P		
5D	±10.24 V	A-D, N-P, E4-E5		
6A	0-10.24 V	B-D, C-E, F-H, K-M, E4-E5		
7D	±5.12 V	A-D, C-E, F-H, N-P, E4-E5		
8A	0-5.12 V	A-D, B-E, J-K, N-P, E4-E5		

ORDERING GUIDE

Normally, the four DACs on each board will be configured for the same voltage range. Coding is shown below:

AC15621A	0-10 V, Binary
AC15622D	±10 V, 2's Complement
AC15623D	±5 V, 2's Complement
AC15624A	0-5 V, Binary
AC15625D	±10.24 V, 2's Complement
AC15626A	0-10.24 V, Binary
AC15627D	±5.12 V, 2's Complement
AC15628A	0-5.12 V, Binary

On special request, some flexibility is available by allowing DACs with different voltage ranges on the same card; however, the following constraints apply: The digital coding chosen, (i.e., binary or two's complement) involves the inversion of the MSB and affects all four DACs simultaneously. Similarly, the selection of the X1.024 ranges (i.e., codes 5D, 6A, 7D, and 8A) also affects all four DACs.

Within these limitations, circuit boards can be configured with a mix of voltage ranges, e.g.; 0-10 V binary and 0-5 V binary, or ±10.24 V, 2's complement and ±5.12 V, 2's complement, etc.

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REV	E.C.O.	DESCRIPTION	DWN	APPL	DATE
EA	4-0160-7116	DELETE C104-904 & R102-902	J.L.	L.J.M.	2-15-78

REVISIONS

REV	ECO	DESCRIPTION	DWN	APPL'S	DATE
2	70617	REVISED PER ECO	EP	L JM	10 1 76

SIZE C — 7424-S — REV 2A

CARD SELECT

(A4) (A5) (A6) (A7) A8 A9 A11 DIG OUT STROBE CLEAR

CUT E7-E8 AND JUMP E6-E7 FOR CLEAR FUNCTION

LOAD PULSE
DATA
CLEAR
REF.
LOAD Ø

DAC 3
OUT 3
RET. SENSE 3
RETURN 3

DAC 2
OUT 2
RET. SENSE 2
RETURN 2

DAC 1
OUT 1
RET. SENSE 1
RETURN 1

DAC Ø
OUT Ø
RET. SENSE Ø
RETURN Ø

ANA. GND.
DIG. GND.

SIGN
UNIPOLAR, E1-E3
BIPOLAR, E2-E3

D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12

Z101 74C174 (1/2)
Z102 74C174
Z103 MN562 MSB LSB

RANGE JUMPERS
SENSE JUMPERS

C105 C106, 62 PF C102 .02 C103 .01 µF
R105 10Ω R104 20K R107 4.99K R106 10K R109 R108 4.99K
A101 499.2Ω R103 100Ω
R109A 1/8 CARBON F.A.

+5 L1 C1 15 µF, 10V DIG GND

RANGE X 1.024 E4-E5
R1 F.A. R2 3.7K R3 1870 R4 953K R5 F.A. R6 6.3K
REFERENCE
CR1 AD-131139
C4 4.7 µF, 35V

+15 L2 C2 4.7 µF, 35V
15 RET C3 4.7 µF, 35V
-15 L3

RANGE	JUMPERS	SIGN	SENSE
+,- 10V	B-D, C-E	E2-E3	F-H, K-M
0-10V	A-D	E1-E3	N-P
+,- 5V	A-D, C-E	E2-E3	F-H, N-P
0-5V	A-D, B-E	E1-E3	J-K, N-P

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS ± DECIMALS ± ANGLES ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

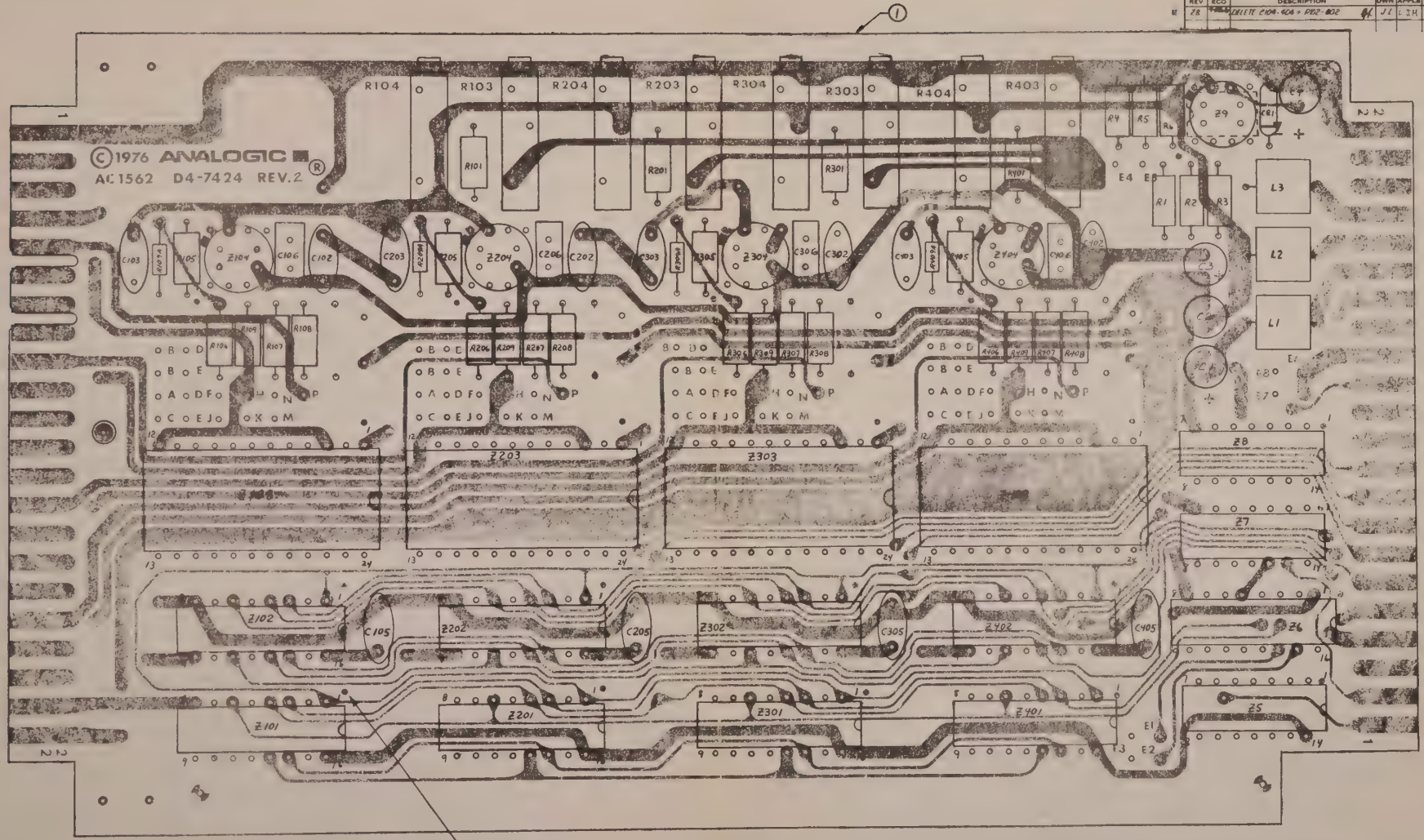
	DRAWN	DATE
	RWH	4-22-76
CHECKED		8-17-76
DESIGNER	RWH	8-17-76
ENGINEER		8-15-76
APPROVED		8/19/76
RELEASED		9/14/76
WEIGHT		

PLO-7424 | AC1562
NEXT ASSY | USED ON
APPLICATION

ANALOGIC WAKEFIELD, MASS. 01880

AC1562
4 CHANNEL, 12 BIT D/A CONVERTER

CODE IDENT NO	SIZE		REV
31814	C	5-7424	2A
SCALE	ACCOUNT NO	SHEET / OF /	



COMPONENT SIDE

NOTES:
1. FOR SCHEMATIC SEE CS-7424.
2. DOTS INDICATES PIN 1 OF INTEGRATED CIRCUITS.
3. ASSEMBLE IN ACCORDANCE WITH 82-1027.

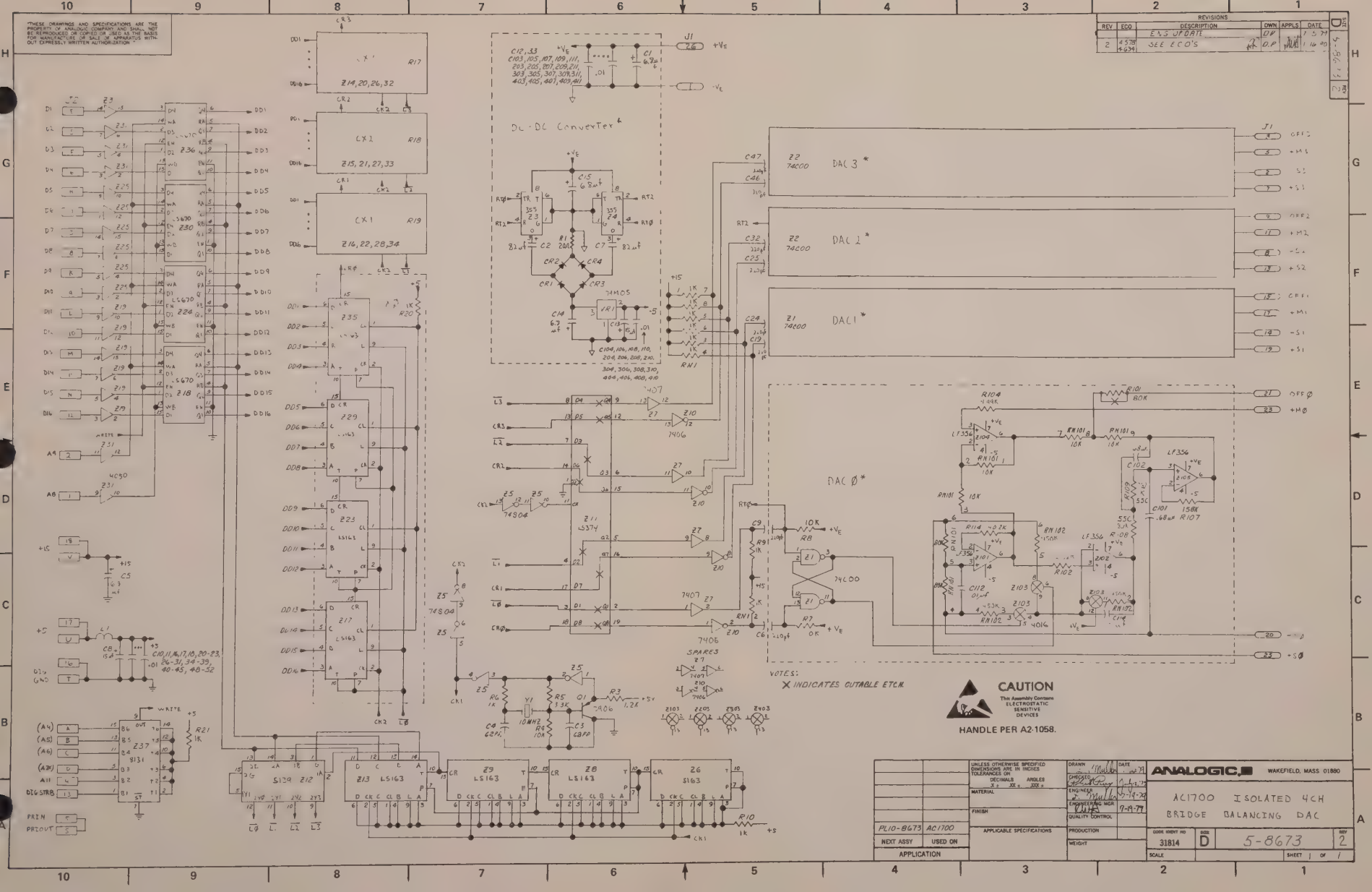
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPD	DATE
2B		DELETE E104-404 + D62-802	AK	JL	2-6-78

D 7-7424 2B

ANALOGIC

ASSEMBLY
AC1562

31814 D 7-1164 2B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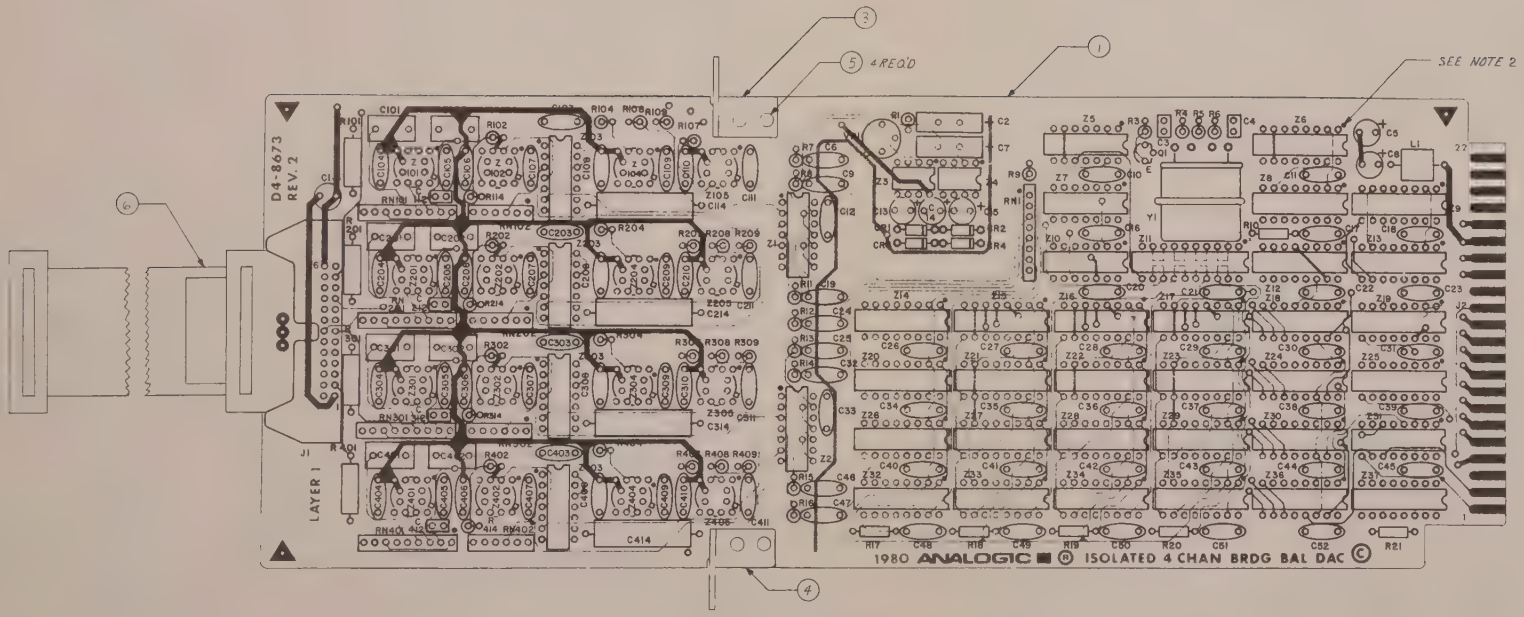
REVISIONS
REV ECO DESCRIPTION OWN APPLS DATE
2 4578 +634 ENG UPDATE SEE ECO'S DV DP 1 16 79
DC-DC Converter
DAC 3 *
DAC 2 *
DAC 1 *
DAC Ø *
74LS04
74LS374
74LS163
74LS00
74LS07
74LS06
74LS05
LF356
VOTES:
X INDICATES CUTABLE ETCH
CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS ANGLES
.X ± .XX ± .XXX ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
PRODUCTION
WEIGHT
DRAWN
CHECKED
ENGINEER
ENGINEERING MGR
QUALITY CONTROL
DATE
PL10-8673 AC1700
NEXT ASSY USED ON
APPLICATION
ANALOGIC WAKEFIELD, MASS 01880
AC1700 ISOLATED 4CH BRIDGE BALANCING DAC
CODE IDENT NO 31814
SIZE D
5-8673
REV 2
SCALE
SHEET 1 OF 1

REVISIONS						
REV	ECO	DESCRIPTION	DWN	APPLS	DATE	
C	4526 4634	SEE E.C.O.'S	PK	DP	1-16-80	

D 7-8673 2



COMPONENT SIDE

NOTES:
1. FOR SCHEMATIC SEE D5-8673.
2. DOT INDICATES PIN 1 OF I.C.'S & R.N.'S.
3. MANUFACTURE PER A2-1040.

CAUTION
Static Sensitive Assembly Contains ELECTROSTATIC SENSITIVE DEVICES

HANDLE PER A2-1058.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS .XX .XXX ANGLES ± MATERIAL FINISH		DRAWN	K. Erickson	5-3-79	ANALOGIC ■ WAKEFIELD, MASS. 01880
		CHECKED	R. FLAHERTY	7-12-79	ASSEMBLY ISOLATED 4 CHAN. BRDG. BAL DAC AC 1700
		ENGINEER	L. MULLER	7-19-79	
		ENGINEERING MGR	R.W. HAVENER	7-19-79	
		QUALITY CONTROL			
PLID-8673 AC 1700	APPLICABLE SPECIFICATIONS A2-1027	PRODUCTION			CODE IDENT NO 31814 SIZE D DWG NO 7-8673 REV 2
NEXT ASSY USED ON		WEIGHT			SCALE 2:1 SHEET
APPLICATION					

AC1814/AC1813

ANALOG OUTPUT FOR AN5400

GENERAL DESCRIPTION

The AC1814, AC1813, is an analog output card for the AN5400 Data Acquisition System. The AC1814 contains two 14 bit digital-to-analog converter modules, with address and control logic, and storage registers. The AC1813 is identical except that the digital-to-analog converter modules are 13-bit units. Both cards feature two 2-bit digital output ports similar to the AC1520 and AC1320.

The AC1814, AC1813 are available with tristate buffers which enable readback of the DAC data registers. This option, designated RB, also enables external input from two 2-bit digital input ports. System inputs, power requirements, mechanical dimensions compatible with AN5400.

SPECIFICATIONS

ACCURACY (@23°C):
Resolution: 14 bits (AC1814), 13 bits (AC1813)
Relative Accuracy: ±0.003% (AC1814), ± 0.006% (AC1813)

ANALOG OUTPUT:
Full scale ranges: ± 10V, ±5V, +10V, +5V
Impedance: Less than 0.1 ohm
Load Current: ±5mA
Load Capacitance: 1000pf (for rated speed)

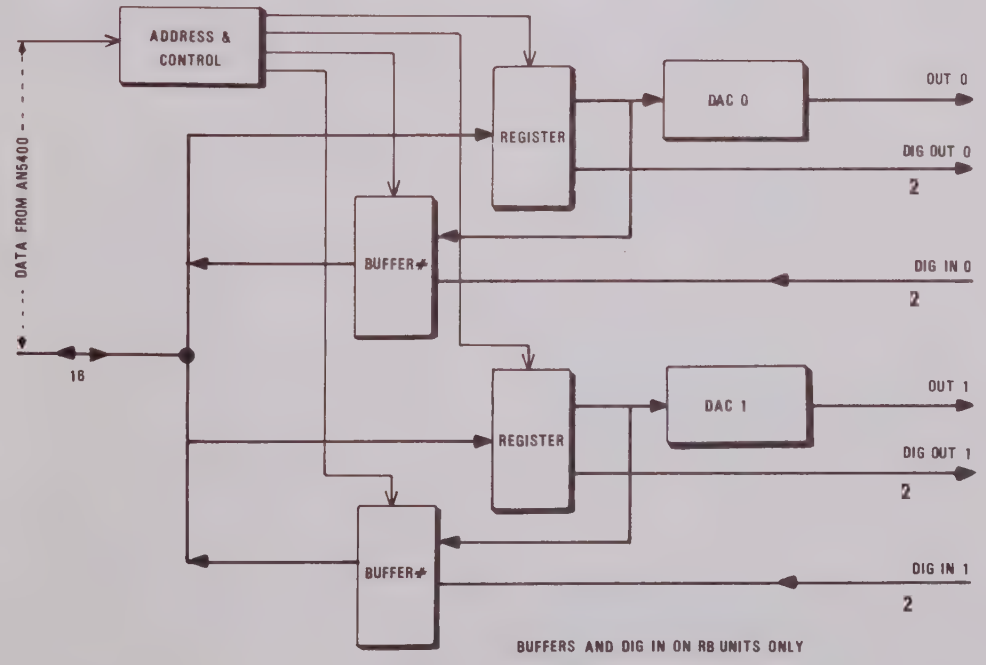
SPEED:
Settling time to 1 LSB: 15μs max.
Slew Rate: 10V/μsec.

STABILITY:
Tempco of Range: 10ppm/°C max.
Tempco of Offset: 10ppm/°C max.
Tempco of Differential Linearity: 3 ppm/°C max.

CALIBRATION ADJUSTMENTS:
Range: ±0.1% FSR
Offset: ±0.05% FSR

DIGITAL OUTPUTS:
CMOS compatible, 2 TTL load drive capability

DIGITAL INPUTS:
10K Pullup to +5 on each input. Threshold = 1.5 to 3.5 volts
CMOS — TTL compatible



AC1814/AC1813 Block diagram

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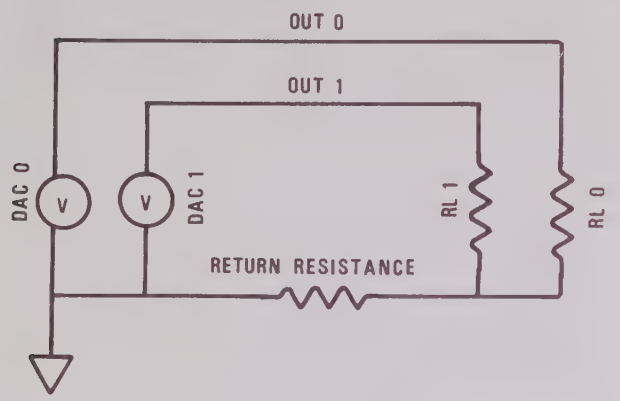
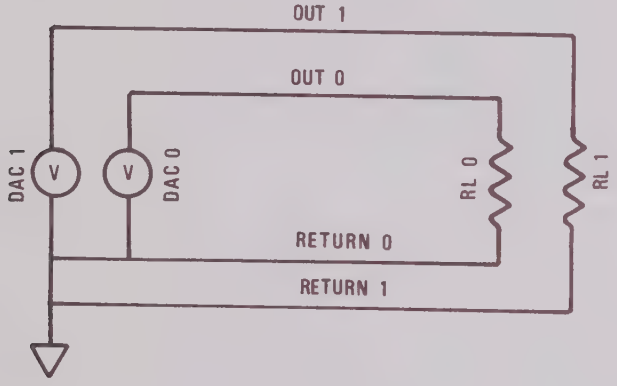
. . . The Digitizers

LOAD CONNECTIONS

When driving true floating loads it is important to use the separate return lines for each DAC. Consider the following example:



Notice that the voltage across RL1 will be changed if the output of DAC 0 changes, because of the common return lead resistance shared by the two loads. The correct way to connect floating loads is as follows:



This use of separate return lines avoids crosstalk between DACs.

DIGITAL OUTPUTS

The AC 1814, 1813 DACs are loaded with 16 bit parallel data in the normal manner described in Chapter 3 of the AN5400 Manual and in the specification for the interface being used. The effect of this data on the card is shown below:

The two bits that are not used for the DAC are available at the user connector for any desired customer function. The AC1813 does not use bit 14, but it is still present in the register.

DIGITAL INPUTS

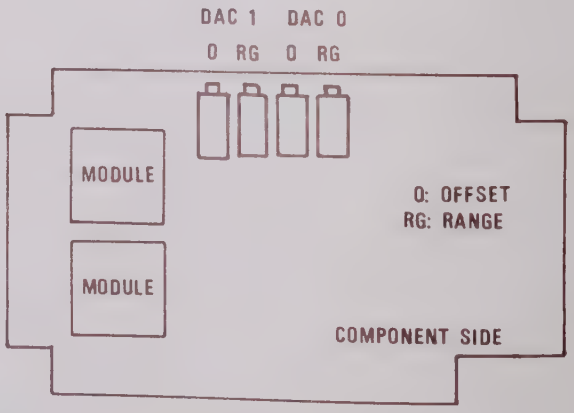
The RB versions of the AC1814, AC1813 DACs, when used in the Master Chassis of the AN5400, will supply digital inputs to the user's computer in the following format:

The two bits not supplied by the DAC register come from the user connector and can read any 5 volt CMOS or TTL signal supplied by the customer. On the AC1813, bit 14 is still in the register and will be readback.

The two digital outputs and two digital inputs with each DAC are totally independent; but if it is desired to read back the digital outputs as digital inputs, note that the pins are conveniently placed across from one another and can be easily bussed together. In this manner, complete equality between the 16 bit output word and the 16 bit input word is achieved.

CALIBRATION INSTRUCTIONS

Calibration of the AC1814, AC1813, when required, consists of adjusting the Offset and Range controls for each DAC. These controls are located across the top edge of the PC card and can be accessed either by the use of an extender card (Analogic AC70) or by removal of the AN5400 top cover. The relative location of the potentiometers is shown in the diagram below.



Connect a precision, high impedance DVM (e.g. Data Precision Model 2540) between the output and return pins of each DAC as it is calibrated. Allow a 5 minute warmup time.

ZERO CALIBRATION

Put the AN5400 into local control; address DAC 0 on the card being calibrated; apply the appropriate data inputs to the card as described in the operating instructions in Chapter 3 of the AN5400 Manual. Apply the data input that will give zero volts output. For a 2's complement DAC, this will be an octal code 000000. For a binary DAC it will be an octal 000000. Adjust the offset potentiometer for zero volts on the DVM.

RANGE CALIBRATION

Address DAC 0. Apply the data code that results in the most positive DAC output voltage. For a binary DAC, this will be octal code 177777. For a 2's complement DAC it will be octal 077777. Adjust the range potentiometer for the correct reading according to the chart below:

AC1814	AC1813
0 to 10V = +9.9994	0 to 10V = +9.9988
±10V = +9.9988	±10V = +9.9976
±5V = +4.9994	±5V = +4.9988
0 to 5V = +4.9997	0 to 5V = +4.9994

Because of a slight interaction, repeat the offset and range adjustments until no further adjustment is required. Repeat the above procedure for DAC1.

Ordering Code:

Normally, the two DACs on each board will be configured for the same output range. Two different ranges may be accommodated if specially ordered from the factory or if altered in the field.

Specify AC181☐-☐-☐

For	
Resolution	
14-bits	4
13-bits	3
D/A with two 2-bit output ports	blank
Digital readback & two 2-bit input ports	RB
Full Scale Ranges	
0–10V binary	1A
±10V 2's complement	2D
±5V 2's complement	3D
0–5V binary	4A

PIN CONNECTIONS (USER)

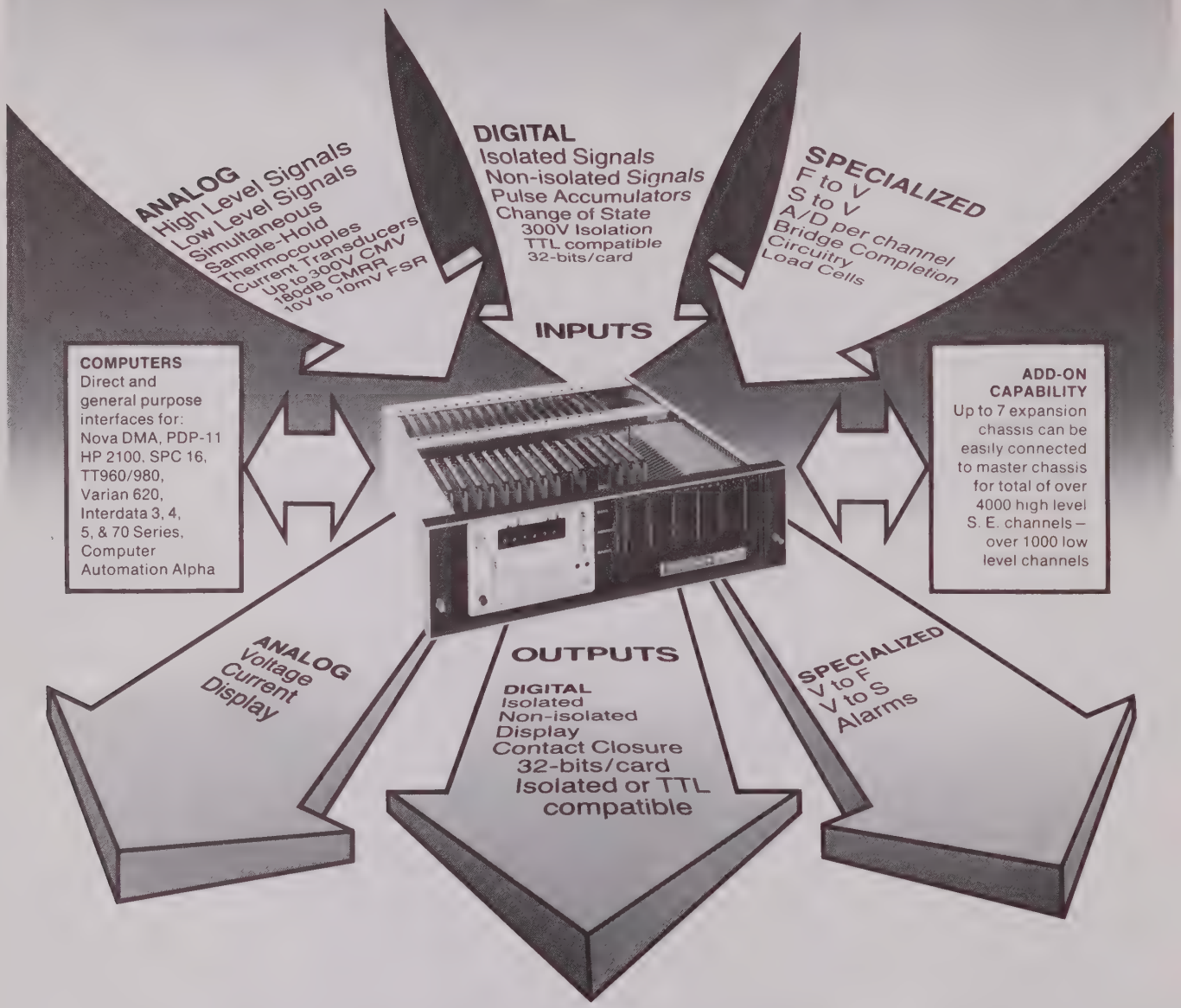
Analog Gnd	A	1	Analog Gnd
0 input 16 (LSB)*	B	2	0 output 16 (LSB)
0 input 15 *	C	3	0 output 15
0 DAC output	D	4	
0 DAC gnd. rtn	E	5	
	F	6	
	H	7	
	J	8	
	K	9	
	L	10	
	M	11	
	N	12	
1 DAC output	P	13	
1 DAC gnd rtn	R	14	
1 input 16 (LSB)*	S	15	1 output 16 (LSB)
1 input 15 *	T	16	1 output 15
	U	17	
	V	18	
	W	19	
	X	20	
Digital Gnd	Y	21	Digital Gnd
Analog Gnd	Z	22	Analog Gnd

* RB UNITS ONLY

SYSTEM ENGINEERS . . .

put yourself in control

WITH ANALOGIC'S AN5400 BUILDING BLOCK DATA ACQUISITION SYSTEM



The AN5400 Installation...

is usually the simplest and most troublefree part of the assembly and proving out of any large system. There are many reasons for this, but chief among them are exhaustive pre-shipment computer-programmed testing to verify specified performance; complete access to all signal and control input/output cabling and input/output modules; generous performance margins in all module designs; and the "stand-alone", self-powered nature of the AN5400.

The Analogic Customer...

has available to him the extensive resources of Analogic's Applications and Field Engineering staffs, including regional Field Managers with direct access to the factory backup. We are always ready to consult on new requirements, upgrading and expansion of existing systems, and major system reconfiguration.

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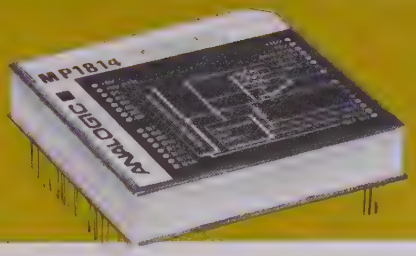

MP1814

High Performance General Purpose

14-Bit D/A CONVERTER

GENERAL DESCRIPTION

The Analogic MP1814 is a premium quality digital-to-analog converter which provides genuine 14-bit resolution, linearity, and stability at only slightly more than 12-bit prices. Every contributing element to the MP1814 Error Budget has been designed and engineered to provide a converter that meets the requirements for economical, high-speed, accurate, and stable 14-bit resolution in high-precision, wide-dynamic-range applications.

PERFORMANCE ACHIEVEMENTS

The MP1814 incorporates high-speed, thermal tracking, monolithic voltage switches; precise, ultra-stable, network resistors; and a reference source servoed to an aged, temperature-compensated precision reference Zener for accurate, stable operation over wide temperature ranges. The MP1814 also includes a high speed voltage amplifier that slews at 10V/μsec and supports the throughput settling time of less than 15μsec for conversion to within ±0.005% of a full 20-volt step.

The versatile MP1814 provides the user with pin-selectable full scale ranges of ±10V, ±5V, +10V, and +5V analog outputs for computer-compatible binary or offset binary input data codes.

The MP1814 small size (2" x 2"), low profile (0.375"), metal case provides RFI and EMI shielding, and encloses a repairable assembly that includes high-quality power supply by-pass capacitors to prevent power supply transients from interfering with conversion performance.

APPLICATIONS

The Analogic MP1814 provides a capability for instrumenting true 14-bit information translation systems at hitherto unobtainable economy. When combined with other Analogic system-compatible modules, the MP1814 delivers value-added accuracy for instrumenting a multitude of wide-dynamic range display and control systems at significantly less cost than that of available instrumentation for comparable performance.

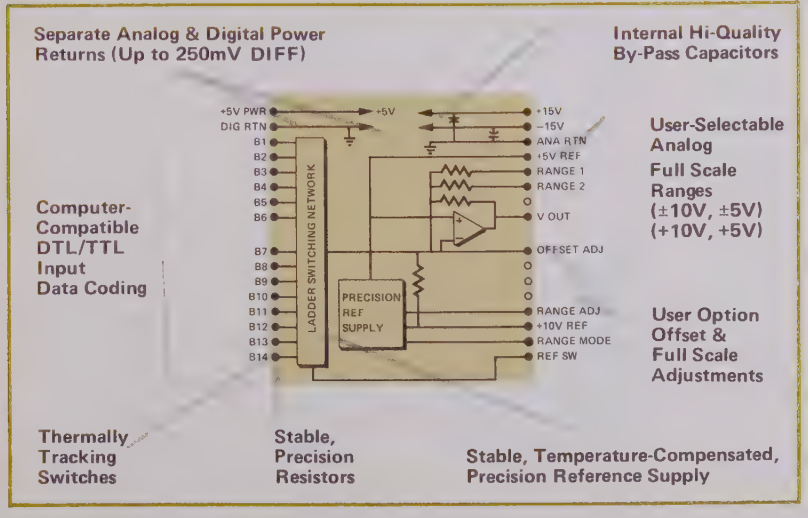

Figure 1. MP1814 Functional Block Diagram

FEATURES

- True 14-bit Accuracy and Linearity
- Maximum Interface Compatibility
  - . . . Selectable ±10V, ±5V, +5V, +10V Output Voltage
  - . . . Positive True Logic Input Coding (TTL Compatible)
- High Speed
  - . . . 15μsec max to 0.005% of 20-volt step
- Separate Digital and Analog Grounds
  - . . . Up to 250mV potential difference
- Guaranteed Monotonicity
  - . . . Differential Linearity within 0.003%
  - . . . Tempco of Differential Linearity 1ppm/°C typ
- Low Profile
  - . . . 0.375" high metal shielding case

APPLICATIONS

- Wide Dynamic Range, Computer Controlled, Industrial Processes
- High Precision CRT Display Systems
- Automated Test Instrumentation
- Waveform Synthesis and Recovery
- High Resolution Information Translation Systems
- Programmable Control Instrumentation (Gain, Offset, etc.)
- High Resolution Oscillographic Recordings

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MP1814 SPECIFICATIONS

DIGITAL INPUTS	
No. of Bits	14
Coding	Binary, Offset Binary Positive "TRUE" Logic
Compatibility	1TTL/Bits 2-14; 2TTL/MSB-1
ANALOG OUTPUT	
Full Scale Ranges	±5V, ±10V, +5V, +10V
Impedance	$< 0.1\Omega$ (DC)
Maximum Load	$2K\Omega \parallel 1000pF$ for rated settling time
INTERNAL REFERENCE OUTPUT	
Voltage	+10V, +5V
Impedance	$< 0.1\Omega$
SPEED	
Settling Time	10μsec typ., 15μsec max for 20-V step to 0.005%
Slew Rate	10V/μsec
ACCURACY	
Absolute Accuracy	±0.006% FSR*
Linearity	±½ LSB (±0.003% FSR)
Differential Linearity	±½ LSB (±0.003% FSR)
Zero Offset	Adjustable to zero

STABILITY	
Diff. Linearity Tempco	1ppm/°C typ., 3.0ppm/°C max
Range (Gain) Tempco	7ppm/°C typ., 10ppm/°C max
Zero Offset Tempco	
Unipolar	5ppm/°C typ., 7.5ppm/°C max
Bipolar	7ppm/°C typ., 10ppm/°C max
Noise	±0.005% FSR p-p (3σ)
Power Supply Sensitivity	±0.0005%/% P.S. Change, nominal
Warm Up Time	5 minutes
POWER SUPPLY GROUNDS	Separate Analog and Digital Grounds; 250mV max allowable difference of potential
POWER REQUIREMENTS	
+15V ±3%	34mA max + Load
−15V ±3%	30mA max + Load
+5V ±5%	35mA max + Load
ENVIRONMENTAL AND PACKAGING	
Operating Temp.	0° to 70°C
Relative Humidity (Non-condensing)	5% to 95%
Size	2" x 2" x 0.375"
Shielding	RFI 6 sides, EMI 5 sides
Storage Temp.	−25°C to +85°C

*Adjustable to ±0.003% with proper adjustment of external trim pots.

COMMENTARY

The trend toward increased resolution in Information Translation and Data Acquisition Systems has created increased demand for 14-bit converters. Until now, most available 14-bit digital-to-analog units have demonstrated poor PERFORMANCE/COST ratios. That is, relatively low-cost 14-bit units have been "extended-bit 12-bit units" and yield 14-bit performance in name only. On the other hand, until the availability of the Analogic MP1814, true 14-bit conversion modules have been offered at only slightly less cost than the very high-priced 15-16-bit converters. Thus, the system designer has been faced with a cost-performance dilemma.

True 14-bit performance within 1 LSB implies a total ERROR BUDGET which does not exceed 0.006% (or 60ppm) of full scale. Clearly, merely adding two least significant input control bits (and appropriate resistor network elements) to a 12-bit unit to provide 14-bit input switching does not improve the 12-bit performance.

The specifications of many 14-bit converters, that are offered at moderate prices, may appear to provide 14-bit performance, but, on closer scrutiny, reveal their 12-bit limitations. For example, a differential linearity specification of +0.005% FSR and a differential linearity stability of 5 ppm/°C provide excellent 12-bit performance (where 0.025% FSR is 1 LSB). However, when these performance specifications are carried over for the nominal 14-bit converter, they are marginal at best. An error of 0.005% (50ppm) is 80% of an LSB, and very little temperature shift (only 2°C) at 5ppm/°C will introduce significant errors, inducing missing codes in the conversion. For the MP1814, the initial differential linearity accuracy of 0.003% (30ppm) allows a temperature variation of 30°C for the typical differential linearity temperature coefficient and 10°C for the maximum temperature coefficient. In addition, the MP1814 specifications are presented without any reservations, such as the phrase "typical @25°C " that appears on a number of competitor data sheets.

Obviously, it is a simple matter to eliminate one or two of the input data bits of a 15 or 16-bit digital-to-analog converter, to obtain a 14-bit unit. Furthermore it may be possible to reduce or omit some in-process and final test and calibration procedures, thereby reducing the cost somewhat. One may thus obtain a 14-bit converter, **but at a high price!**

CALIBRATION

Linearity and relative accuracy for 14-bit performance are designed in. Absolute accuracy calibration may be set externally as shown in Figure 2 and described below.

Offset Adjustment

The analog output is adjusted for zero, or other desired offset, by connecting R1 (10-turn 20kohm potentiometer) and R3 (2 megohms) as shown in Figure 2. Use thermally stable components of 50ppm/°C or better, and keep the connection leads as short as possible to maintain the MP1814 performance integrity of 14-bit conversion.

After making the required connections, (Table 2) apply the appropriate "ZERO" code (See Table 1), and adjust R1 for 0.0000 volts output.

Range Adjustment

The MP1814 analog output may be calibrated for the desired full scale range by connecting R2 (10-turn 20kohm potentiometer) and R4 (1 megohm) as shown in Figure 2. (See stability and lead length requirements described above.) Apply the full scale code as indicated in Table 1, and adjust R2 for the appropriate full scale voltage output.

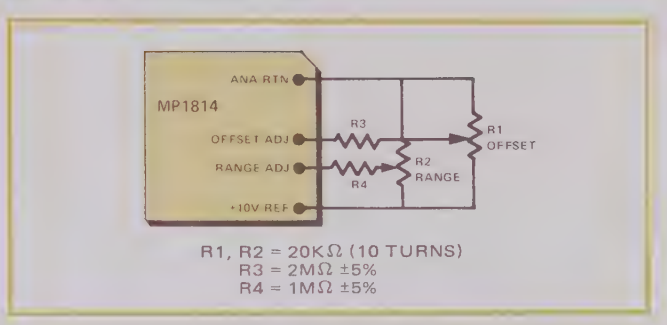


Figure 2. Connecting External Adjustment Potentiometers for MP1814 OFFSET and RANGE

CODE	UNIPOLAR (Binary)		BIPOLAR (Offset Binary)	
	0 to +10V	0 to +5V	±10V	±5V
111 111 111 111 11	9.9994	4.9997	9.9988	4.9994
100 000 000 000 00	5.0000	2.5000	0.0000	0.0000
000 000 000 000 01	0.0006	0.0003	−9.9988	4.9994
000 000 000 000 00	0.0000	0.0000	−10.0000	−5.0000

Table 1. MP1814 Coding Translation Table

FOR FSR ↓	CONNECT		
	RANGE MODE TO ↓	RANGE 1 TO ↓	RANGE 2 TO ↓
±10V	REF SW	+5V REF	ANA RTN
±5V	REF SW	+5V REF	V_{OUT}
+10V	ANA RTN	ANA RTN	V_{OUT}
+5V	ANA RTN	V_{OUT}	V_{OUT}

Table 2. Connection Matrix for Full Scale Outputs

AN1814M (CARD-MOUNTED MP1814)

Analogic's AN1814M is a complete digital-to-analog converter in a standard PC-card configuration. It includes the low-profile MP1814 Modupac and the calibration circuitry as described earlier, instrumented with precise, stable resistance elements to maintain the accuracy and stability of 14-bit performance.

The AN1814M may be ordered with storage registers (AN1814ML) for increased versatility in user information translation systems. The registers perform a parallel-to-parallel bit transfer under control of a transfer STROBE signal. When the STROBE goes HIGH, the input data bits are transferred through the registers to the MP1814 inputs. Input loading of each bit is 1 unit load (TTL 40μA high and 1.6mA low), while the STROBE loading is 2 unit loads. Timing relationships for changing data input bits and STROBE are shown in Figure 3.

The 1814ML terminals are configured so that data inputs may be connected directly to the MP1814, even when the registers are not installed.

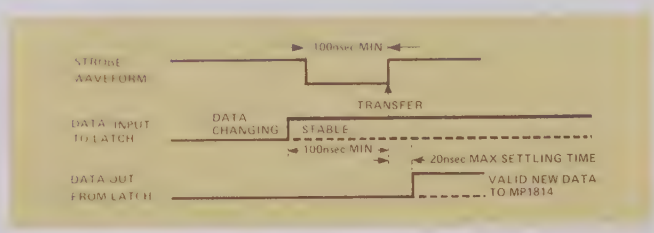


Figure 3. Strobe and Data Input Timing

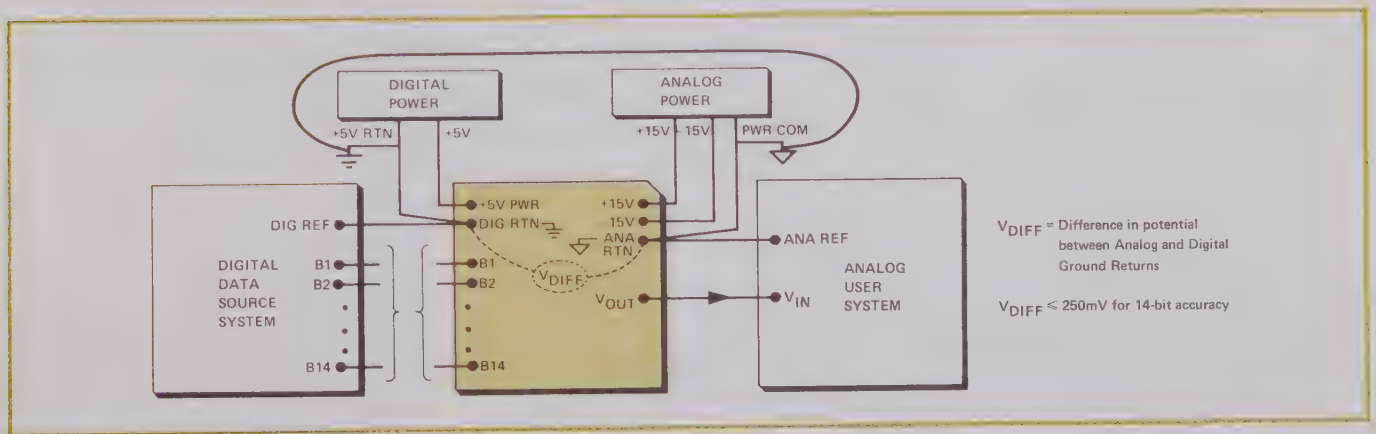


Figure 4. MP1814 in System Configuration, showing Connections of Data Inputs, Analog Output, and Power Sources. Connect Analog Power Return to Digital Power Return as shown (with short, heavy duty conductor) to keep Digital IR Transients from ANA Signal.

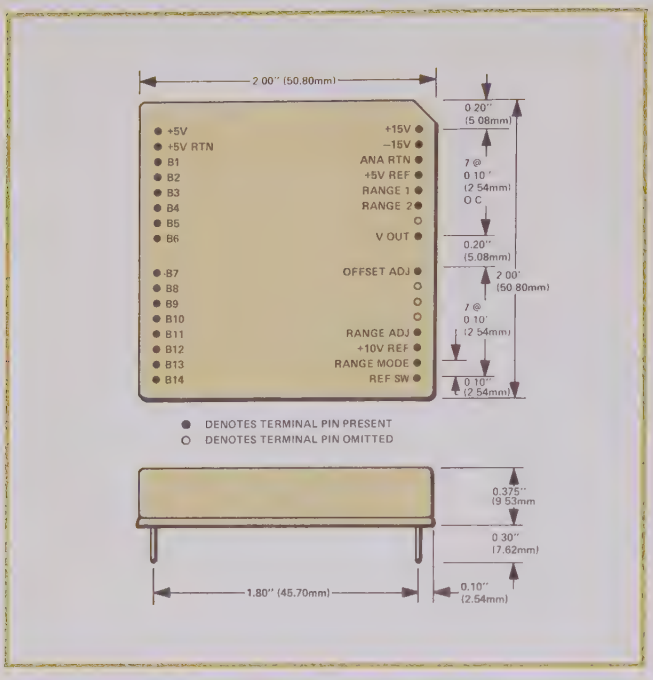


Figure 5. MP1814 Outline Dimensions

ORDERING GUIDE

Simply Specify ☐

For	Enter
14-Bit Modupac	MP1814
MP1814 on P.C. card	AN1814M* — ☐ — ☐

For FS Range	Enter
0 to +10V	1
–10V to +10V	2
–5V to +5V	3
0 to +5V	4

For Input Code	Enter
Binary or Offset Binary	A
** 1's Complement	C
** 2's Complement	D

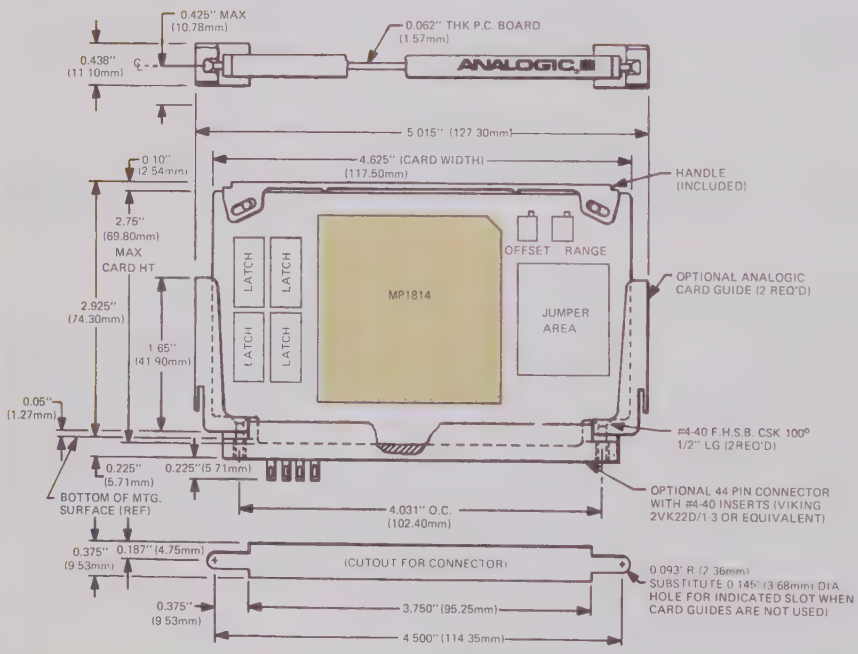
AN Version Only

*Includes OFFSET and RANGE ADJ potentiometers. To include optional latches, add "L" to basic part number.

For Example
AN1814ML-2-C is a card-mounted MP1814 with input storage latches; connected for ±10V full scale range and 1's complement input code.

****NOTE:** To configure MP version for a 1's complement or 2's complement input, MSB must be inverted. When ordering AN types, inversion is included on P.C. Card.

OUTLINE DRAWING



PIN DESIGNATIONS

+5V REF	A	1	+10V REF
	B	2	STROBE**
	C	3	
	D	4	
*B14 OUT	E	5	B14 IN
*B13 OUT	F	6	B13 IN
*B12 OUT	H	7	B12 IN
*B11 OUT	J	8	B11 IN
*B10 OUT	K	9	B10 IN
*B9 OUT	L	10	B9 IN
B8 IN	M	11	+5V IN
*B8 OUT	N	12	+5V RTN
*B7 OUT	P	13	B7 IN
*B6 OUT	R	14	B6 IN
*B5 OUT	S	15	B5 IN
*B4 OUT	T	16	B4 IN
*B3 OUT	U	17	B3 IN
*B2 OUT	V	18	B2 IN
ANA RTN	W	19	ANA RTN
*B1 OUT	X	20	–15V
(MSB)B1 IN	Y	21	+15V
DAC OUT	Z	22	DAC OUT

*LATCH OUTPUTS, use as Direct Inputs if LATCH Register is not installed

**Data Transfer control signal, see Fig. 6.

Figure 6. AN1814 Outline Drawing, Mounting Dimensions and PC-Board Edge Connector.

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REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPL'D	DATE
1A	4010B 4011B	SEE E.C.O.'S	J.L.	J.M.	2-15-78
2	4-281	SEE E.C.O.'S	J.L.	J.M.	6-2-80

SIZE C — 5-7426 — REV 2

CLEAR 14

Z2 74C174 · Z3 80C97 · Z5 74C174 · Z6 80C97 · Z9 74C174 · Z10 80C97 · Z13 74C174 · Z14 80C97 · Z16 74C174 · Z17 80C97 · Z20 74C174 · Z21 80C97

Z7 74C10 · Z11 4049 · Z8 4050 · Z12 4050 · Z15 4050 · Z19 4050

M1 MP18XX: 20K R11, R12 20K, 499K R9, 1M R10; RNG ADJ, OFFSET, V OUT, ANA RTN, RNG 2, RNG 1, +5 REF, REF SW, R MODE, +5RTN; OUTPUT B, RTN B, DIG. GND

M2 MP18XX: R7 20K, 499K R8, 1M R6; RNG ADJ, OFFSET, V OUT, ANA RTN, RNG2, RNG1, +5 REF, REF SW, R MODE, +5RTN; OUTPUT A, RTN A, ANA GND

CR1 IN4148 · CR2 IN4148

C6 4.7µf · C7 4.7µf

R1 R2 R3 R4 10K

PORT B: 2', 2°, RB2', RB2° · PORT A: RB2°, RB2', 2°, 2'

DIG. STROBE IN · DEG. · A0 · (A6) · (A5) · (A4) · (A7) · A11

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES · TOLERANCES ON FRACTIONS DECIMALS ANGLES

MATERIAL · FINISH · APPLICABLE SPECIFICATIONS

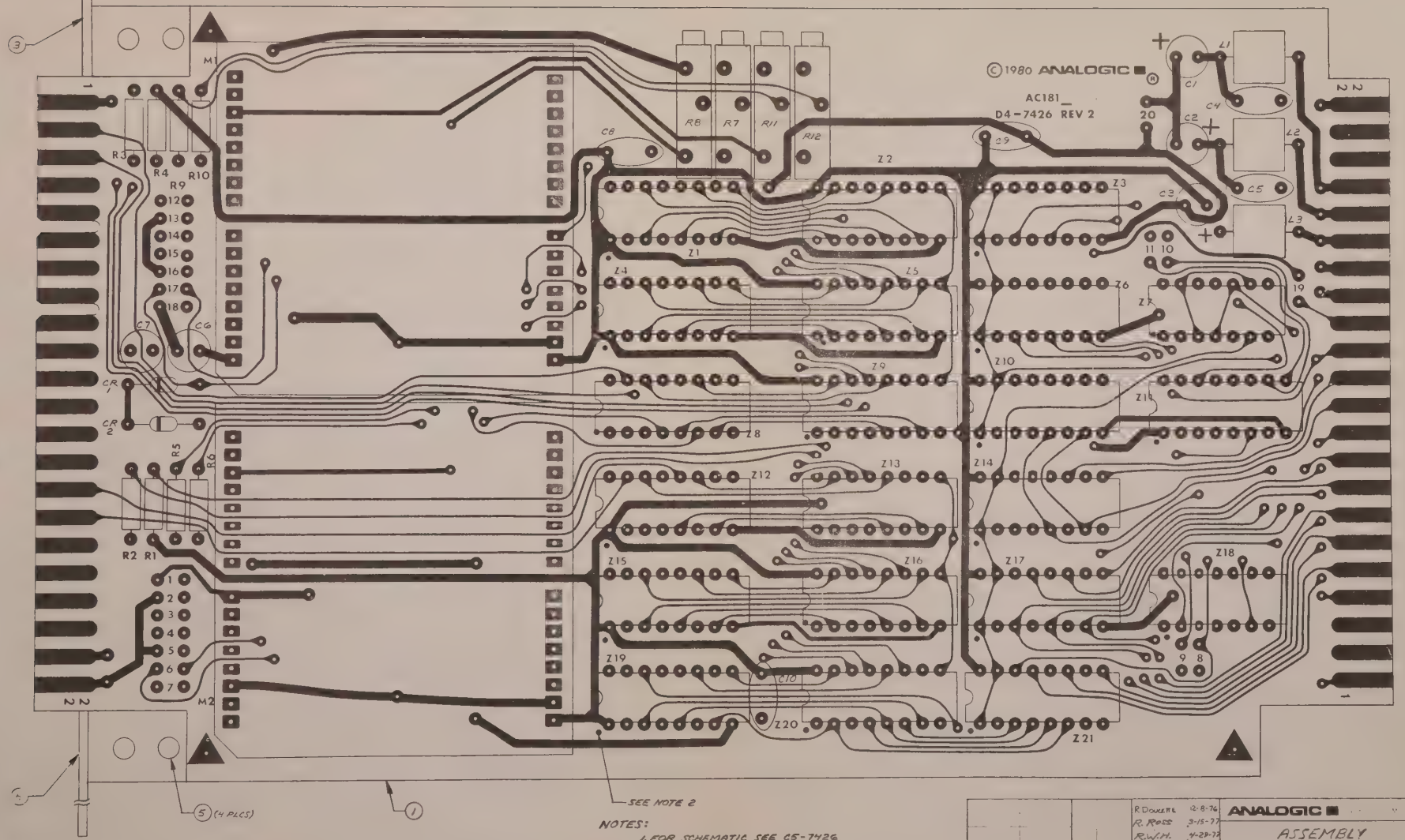
DRAWN	L. J. MULLER	DATE 11-17-76
CHECKED		3-15-77
DESIGNER		4-28-77
ENGINEER		4-28-77
APPROVED		5/1/77
RELEASED		5/4/77
WEIGHT		

ANALOGIC — WAKEFIELD, MASS. 01880

SCHEMATIC
DUAL DAC OUTPUT MODULE
AC1813/14

PL10-7426	AC1813/14
NEXT ASSY	USED ON
APPLICATION	

CODE IDENT NO 31814 · SIZE C · 5-7426 · REV 2 · SCALE — · ACCOUNT NO — · SHEET 1 OF 1



COMPONENT SIDE

NOTES:
1. FOR SCHEMATIC SEE C5-7426
2. DOT INDICATES PIN 1 OF I.C.'S
3. ASSEMBLE IN ACCORDANCE WITH A2-1027

	R Doucette	12-8-76
	R. Ross	3-15-77
	R.W.H.	4-29-77
	R. W.H.	4-29-77
	R.P.	5-17-77
PL10-7426, AC1813/14	R. Peake	5-21-77

ANALOGIC ■

ASSEMBLY
DUAL DAC OUTPUT MODULE
AC1813/14

31814 | D | 7-7426 | 2

W.B. WILE 4/6/80

AC1900 SERIES

D/A CONVERTERS FOR ANDS5400

GENERAL DESCRIPTION

The AC1900 Series of D/A converters incorporates Analogic standard MP1900 Modules mounted on a motherboard for the ANDS5400. Careful design techniques preserve the superb analog characteristics of the module. For detailed analog information consult Analogic Bulletin No. 16-100027 for the standard MP1913, MP1914, MP1915, and MP1916 or Analogic Bulletin No. 16-100043 for information on the temperature-controlled MP1914TC, MP1915TC, or MP1916TC.

PHYSICAL DESCRIPTION

The AC1900 board holds one module which has been mounted upsidedown on the board to eliminate interaction between analog and digital signals. The range and offset adjustments, which are clearly labeled on the module, are used for calibration of the unit, following the procedure outlined in the above bulletins. These controls may be reached without withdrawing the card from the chassis by removing the bottom cover from the ANDS5400 or by utilizing the AC70 Card Extender. Output pin assignments are shown in Table 1.

OPERATION

The digital addressing and data loading of the AC1900 conform to the standard techniques employed in the ANDS5400. Readback allows the computer controlling the system to interrogate the data that was previously loaded into the D/A register. If the D/A converter has less than 16 bits, the board is configured so that the unused LSB's are read back as zeros.

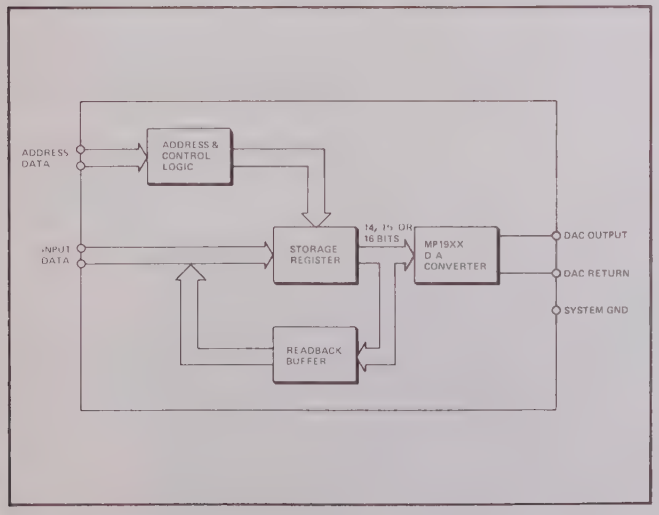


Fig. 1. Functional Block Diagram of AC1900 Series D/A Converter Mother Board.

Table 1
AC19XX User Pin Assignments

ANALOG GROUND - A	1-ANALOG GROUND
B	2
C	3
DAC OUTPUT - D	4
(Analog Gnd) DAC Return - E	5
F	6
H	7
J	8
K	9
L	10
M	11
N	12
P	13
R	14
S	15
T	16
U	17
V	18
W	19
X	20
Y	21
ANALOG GROUND - Z	22-ANALOG GROUND

ADDRESSING

The address structure of the ANDS5400 provides complete flexibility of configuration and installation. Table 2 details the addresses of devices installed in a given enclosure. To determine the absolute address of this device, simply add the address indicated below to the enclosure address in the Digital Output Mode (See ANDS5400 Manual).

Table 2
Address Locations (Octal).

J1	0	J9	40
J2	4	J10	44
J3	10	J11	50
J4	14	J12	54
J5	20	J13	60
J6	24	J14	64
J7	30	J15	70
J8	34	J16	74

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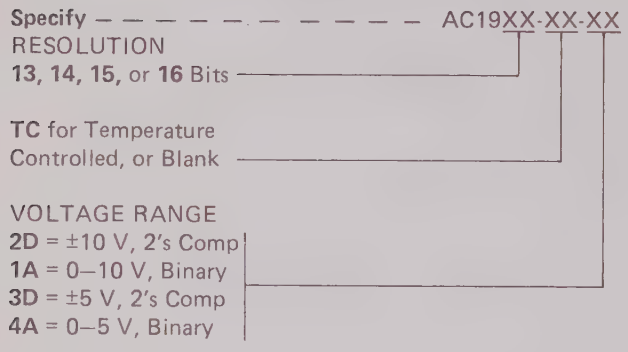
Table 3

Full-Scale Jumper Configurations.*

1A	0-10 V	13, 16, 17	Binary	9
2D	±10 V	13, 15, 17, 18	2's Complement	10
3D	±5 V	13, 16, 17, 18		
4A	0-5 V	13, 12, 16, 17		

*See Schematic C5-7427.

ORDERING GUIDE



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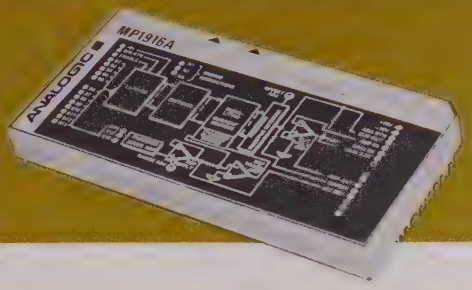

1900A Series

Very High Speed
13, 14, 15 & 16 Bit
D/A CONVERTERS

DESCRIPTION

The Analogic 1900A Series of 13- to 16-bit digital-to-analog converters provides extremely high conversion speeds, superior linearity and absolute accuracy, unequaled thermal stability, and maximum interface compatibility. These uniquely engineered converters, presently unsurpassed in performance, offer true 13 to 16 binary-bit resolution at fast settling times to meet the most exacting industrial and instrument D/A requirements, where high reliability, time and temperature stability and economical cost are critical.

Completely self-contained within a fully shielded low-profile module, the 1900A Series converters include input storage registers, monolithic current switches, a matched precision-weighted resistor network, an output voltage amplifier, a voltage reference supply, externally adjustable internally mounted gain and offset potentiometers, and pin-selectable current or voltage output. (See Figure 1.) Incorporating a state-of-the-art advanced concept design, the 1900A Series converters are eminently qualified for a breakthrough performance in modern high-speed data translation systems.

PERFORMANCE

The 1900A Series converters accept standard binary and 2's complement digital input codes at DTL/TTL compatible levels; provide standard analog output full scale voltages of ±5V, ±10V, +5V and +10V; provide analog output full scale currents of ±2 milliamperes bipolar and 0 to −4 milliamperes unipolar; and operate from external ±15 VDC and +5VDC supplies and an internal reference of +6.5VDC.

Featuring a linearity of 0.001% FSR and an absolute accuracy of 0.002% FSR, the prestigious 1916A 16-bit D/A converter possesses a settling time of 1.5μs to within 1 LSB for a full scale input step in the current mode. In the voltage mode, a settling time of 10μs is obtainable using the internal output amplifier. Relatively noise-free operation from DC to 1 MHz is inherent for all four series converters. Pacesetting thermal stabilities of less than 3ppm/°C, under all converter operating conditions, assure reliable and long-term performance.

IMPLEMENTATION

The 1900A Series converters deliver value-added performance for instrumenting a multitude of wide dynamic range display and control systems, such as precision incremental displays, automated semiconductor testers, automatic typesetters, frequency synthesizers, and nuclear reactor controls, at significantly less cost than competitive converters presently available.

Packaged in a metal case for protection against harsh environments, the 1900 A Series converters can plug directly into a double 22-pin connector (AN card-mounted configuration) or can be soldered to a PC card (MP module configuration). Since the locations of the gold-plated pins are standardized for each configuration, direct interchangeability applies to all four converters in the 1900A Series.

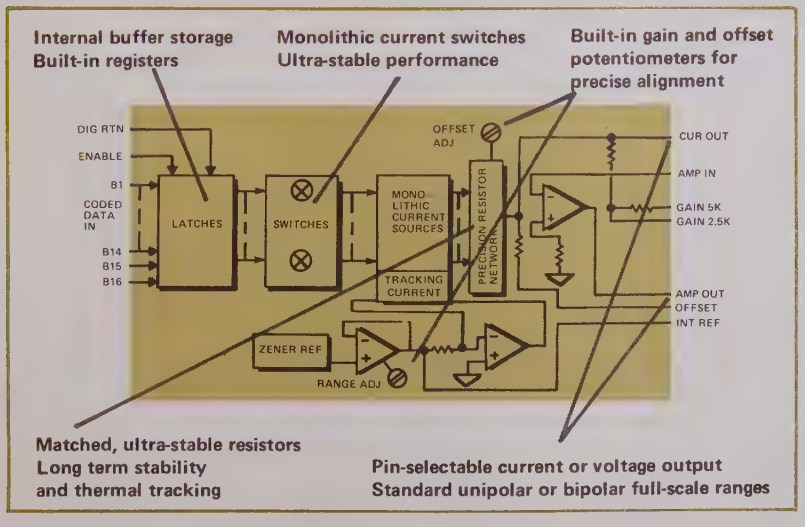

Figure 1. MP1916A Functional Block Diagram

FEATURES

- Up to 16-Bit Resolution.
- Linearity within 0.001% FSR.
- Absolute Accuracy within 0.002% FSR.
- Settling Time within 1.5μs.
- Linearity and Gain Tempco's of 2ppm/°C.
- Pin-Selectable Performance Options
- Self-Contained Registers and Voltage Reference.
- Ultra-Stable Operation.
- Economical Cost.
- Thermally Stabilized Gain and Offset.

APPLICATIONS

- Precision Incremental CRT Displays.
- Nuclear Reactor Controls.
- Automated Semiconductor Testing.
- Waveform Synthesis.
- Automated Typesetting.

NOTE: For all inclusive 1ppm/°C MAXIMUM STABILITY, 14- through 16-bit resolution, send for new 1900TC Series Brochure.

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1900A SERIES SPECIFICATIONS

PARAMETER	MP1916A	MP1915A	MP1914A	MP1913A
DIGITAL INPUT				
Enable	32 loads	32 loads	32 loads	32 loads
DTL/TTL Compatible	2 loads	2 loads	2 loads	2 loads
Number of Bits	16	15	14	13
Input Codes	Binary, 2's complement (pin selectable)	Binary, 2's complement (pin selectable)	Binary, 2's complement (pin selectable)	Binary, 2's complement (pin selectable)
ANALOG OUTPUT				
Current Mode				
Full Scale Range	−2mA to +2mA, bipolar 0 to −4mA, unipolar	−2mA to +2mA, bipolar 0 to −4mA, unipolar	−2mA to +2mA, bipolar 0 to −4mA, unipolar	−2mA to +2mA, bipolar 0 to −4mA, unipolar
Impedance	1.25kΩ, bipolar 2kΩ, unipolar	1.25kΩ, bipolar 2kΩ, unipolar	1.25kΩ, bipolar 2kΩ, unipolar	1.25kΩ, bipolar 2kΩ, unipolar
Voltage Compliance	±1V max.	±1V max.	±1V max.	±1V max.
Voltage Mode				
Full Scale Range	±10V, ±5V, 0 to +10V, 0 to +5V (pin selectable)	±10V, ±5V, 0 to +10V, 0 to +5V (pin selectable)	±10V, ±5V, 0 to +10V, 0 to +5V (pin selectable)	±10V, ±5V, 0 to +10V, 0 to +5V (pin selectable)
Impedance	0.1Ω @ dc	0.1Ω @ dc	0.1Ω @ dc	0.1Ω @ dc
Load Current	±5mA (includes feedback current)	±5mA (includes feedback current)	±5mA (includes feedback current)	±5mA (includes feedback current)
INTERNAL REF. OUTPUT				
Voltage	6.5V ±0.3% (proportional to range control)	6.5V ±0.3% (proportional to range control)	6.5V ±0.3% (proportional to range control)	6.5V ±0.3% (proportional to range control)
Output Impedance	0.1Ω	0.1Ω	0.1Ω	0.1Ω
Current Load	1mA max.	1mA max.	1mA max.	1mA max.
SPEED				
Current Mode				
Settling Time to 1 LSB (Full Scale Step)	1.0μs typ. 1.5μs max.	0.8μs typ. 1.2μs max.	0.6μs typ. 1.0μs max.	0.6μs typ. 1.0μs max.
Voltage Mode (Internal Amp)				
Settling Time to 1 LSB	10μs typ., 20μs max.	10μs typ., 17μs max.	10μs typ., 15μs max.	10μs typ., 15μs max.
Slew Rate	2V/μs	2V/μs	2V/μs	2V/μs
ACCURACY (@ 23°C)				
Linearity	0.001% FSR	0.0015% FSR	0.003% FSR	0.006% FSR
Absolute Accuracy	0.002% FSR	0.004% FSR	0.006% FSR	0.01% FSR
STABILITY				
Current and Voltage Modes				
Tempco of Reference	2ppm/°C typ. 3ppm/°C max.	2ppm/°C typ. 3ppm/°C max.	2ppm/°C typ. 3ppm/°C max.	3ppm/°C typ. 5ppm/°C max.
Tempco of Linearity	1ppm/°C typ. 2ppm/°C max.	1ppm/°C typ. 2ppm/°C max.	1ppm/°C typ. 2ppm/°C max.	1ppm/°C typ. 2ppm/°C max.
Tempco of Gain	2ppm/°C typ. 3ppm/°C max.	2ppm/°C typ. 3ppm/°C max.	2ppm/°C typ. 3ppm/°C max.	3ppm/°C typ. 6ppm/°C max.
Current Mode				
Tempco of Offset	1ppm/°C max., unipolar 2ppm/°C max., bipolar	1ppm/°C max., unipolar 2ppm/°C max., bipolar	1ppm/°C max., unipolar 2ppm/°C max., bipolar	1ppm/°C max., unipolar 3ppm/°C max., bipolar
Voltage Mode				
Tempco of Offset	2ppm/°C max., unipolar	2ppm/°C max., unipolar	2ppm/°C max., unipolar	6ppm/°C max., unipolar
Power Supply Sensitivity	5ppm FSR/% change in dc voltage	5ppm FSR/% change in dc voltage	5ppm FSR/% change in dc voltage	5ppm FSR/% change in dc voltage
NOISE (3σ)				
DC to 1 MHz	0.0015% FSR p-p	0.0015% FSR p-p	0.0015% FSR p-p	0.0030% FSR p-p
DC to 60 Hz	50μV p-p (0.00025% FSR)	50μV p-p (0.00025% FSR)	50μV p-p (0.00025% FSR)	50μV p-p (0.00025% FSR)
DIGITAL CONTROL*				
Enable Input	TTL compatible (high = enable)	TTL compatible (high = enable)	TTL compatible (high = enable)	TTL compatible (high = enable)
Loading	32 loads (MP Series) 1 load (AN Series)	32 loads (MP Series) 1 load (AN Series)	32 loads (MP Series) 1 load (AN Series)	32 loads (MP Series) 1 load (AN Series)
POWER SUPPLY				
+15V ±3%	35mA typ. + load current	35mA typ. + load current	35mA typ. + load current	35mA typ. + load current
−15V ±3%	35mA typ. + load current	35mA typ. + load current	35mA typ. + load current	35mA typ. + load current
+5V ±5%	180mA typ.	180mA typ.	180mA typ.	180mA typ.
ENVIRONMENTAL & PACKAGING				
Storage & Operating Temperature	0°C to +60°C	0°C to +60°C	0°C to +60°C	0°C to +60°C
Relative Humidity	5% to 95%, non-condensing	5% to 95%, non-condensing	5% to 95%, non-condensing	5% to 95%, non-condensing
Warmup Time	5 min. to spec. accuracy	5 min. to spec. accuracy	5 min. to spec. accuracy	5 min. to spec. accuracy
Fault Protection	Output may be shorted to ground indefinitely without damage	Output may be shorted to ground indefinitely without damage	Output may be shorted to ground indefinitely without damage	Output may be shorted to ground indefinitely without damage
Size	4" x 2" x 0.375" (101.6 x 50.8 x 9.5mm)	4" x 2" x 0.375" (101.6 x 50.8 x 9.5mm)	4" x 2" x 0.375" (101.6 x 50.8 x 9.5mm)	4" x 2" x 0.375" (101.6 x 50.8 x 9.5mm)
Shielding	RFI 6 sides; EMI 5 sides	RFI 6 sides; EMI 5 sides	RFI 6 sides; EMI 5 sides	RFI 6 sides; EMI 5 sides

*See Timing Diagram.

MP CONFIGURATION

The 1900A Series of 13- to 16-bit D/A Converters is factory equipped to permit user selection of any of the standard performance options. These selections are accomplished by making appropriate pin connections externally at the module pins of the MP configurations.

Operation for binary, offset binary, or two's complement input code, voltage or current output mode, and the full-scale output range are determined by making the pin connections specified in Figure 2.

When using the current output mode, the built-in voltage amplifier is available for other system applications. However, if not used, the amplifier voltage output should be connected to AMP IN, to prevent possible no-load amplifier oscillations from coupling to the current output signal.

AN CONFIGURATION

Selection of performance options for the AN card-mounted configuration is made by connecting jumpers on the PC Board. The converter output, whether operating in the voltage or current mode, appears at pins 22 and Z on the PC board connector, and is available for a feedback connection as shown in Figure 5. The necessary jumpers are identified in Figure 2 and are shown in Figure 5. Care should be taken to check the jumpers after installation.

Figure 2. Mode and Full-Scale Range Jumper Connections ▶

OUTPUT AND CODING REQUIRED		JUMPERS: PIN JUMPERS ON MODULE	JUMPERS: ADDITIONAL JUMPERS FOR AN VERSION
0 TO 4mA			A4 TO J1
−2mA TO +2mA		OFFSET (A12) TO INT REF (A13)	A4 TO J1
±10V	INTERNAL AMP	CUR OUT (A4) TO AMP IN (A5), GAIN 5K (A6) TO AMP OUT (A11), OFFSET (A12) TO INT REF (A13)	A11 TO J1
±10V	EXTERNAL AMP	CUR OUT (A4) TO (−IN*) GAIN 5K (A6) TO (O/P*) OFFSET (A12) TO INT REF (A13)	A4 TO J1 A6 TO J2
±5V	INTERNAL AMP	CUR OUT (A4) TO AMP IN (A5), GAIN 2.5K (A7) TO AMP OUT (A11), OFFSET (A12) TO INT REF (A13)	A11 TO J1
±5V	EXTERNAL AMP	CUR OUT (A4) TO (−IN*) GAIN 2.5K (A7) TO (O/P*) OFFSET (A12) TO INT REF (A13)	A4 TO J1 A7 TO J2
+10V	INTERNAL AMP	CUR OUT (A4) TO AMP IN (A5) GAIN 2.5K (A7) TO AMP OUT (A11)	A11 TO J1
+10V	EXTERNAL AMP	CUR OUT (A4) TO (−IN*) GAIN 2.5K (A7) TO (O/P*)	A4 TO J1 A7 TO J2
+5V	INTERNAL AMP	CUR OUT (A4) TO AMP IN (A5) GAIN 2.5K (A7) TO AMP OUT (A11), GAIN 5K (A6) TO CUR OUT (A4)	A11 TO J1
+5V	EXTERNAL AMP	CUR OUT (A4) TO (−IN*) GAIN 2.5K (A7) TO (O/P*) GAIN 5K (A6) TO CUR OUT (A4)	A4 TO J1 A7 TO J2
UNIPOLAR BINARY OR OFFSET BINARY		N1 TO N2	
TWO'S COMPLEMENT		N3 TO N2	

NOTE The (+IN*) terminal of the external op amp should be connected to the ANA RTN Pin (A3) of the MP1916 via a resistor (1.2KΩ).
*Connection on external op. amp.

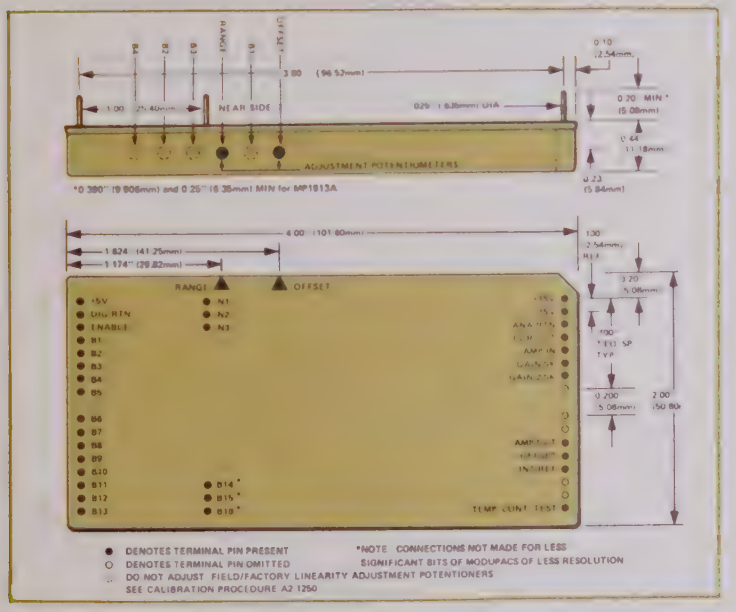


Figure 3. MP19XXA Outline Drawing and Pin Locations

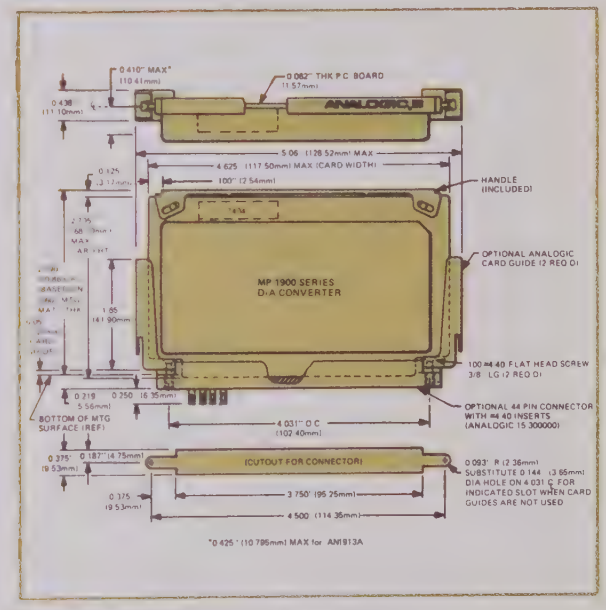

ANALOGIC
MP 1900 SERIES
D-A CONVERTER
HANDLE (INCLUDED)
OPTIONAL ANALOGIC CARD GUIDE (2 REQ'D)
OPTIONAL 44 PIN CONNECTOR WITH #4-40 INSERTS (ANALOGIC 15 300000)
BOTTOM OF MTG SURFACE (REF)
(CUTOUT FOR CONNECTOR)
*0.425" (10.795mm) MAX for AN1913A

Figure 4. AN19XXA Outline Drawing

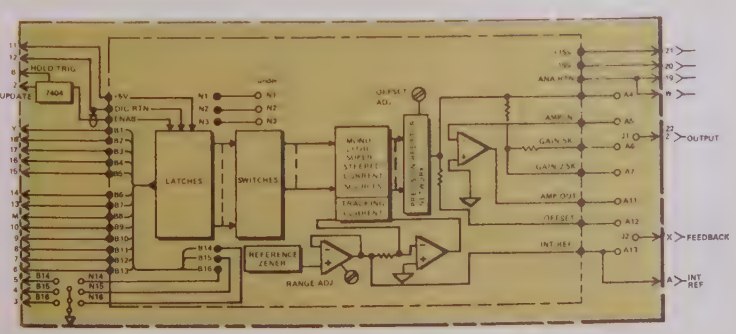
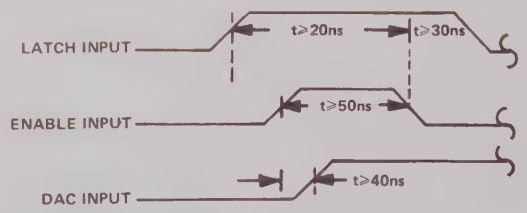


Figure 5. AN1916A Jumper Terminals



Typical Timing Diagram For Any Bit.

Data present at the latch input is transferred to the DAC input when the enable line goes high, and follows the data as long as the enable line remains high. When the enable goes low, the information that was present just prior to the time the transition occurred is retained.

MP1916A DIGITAL INPUT DATA CODING				
FORMAT	INPUT CODE MSB (for 16 bits)** LSB	I_{OUT} Milliamperes* 1913	1914	1915	1916
Unipolar Binary	1111 1111 1111 1111	−3.99950	−3.99975	−3.99988	−3.99994
	0000 0000 0000 0000	0.00000	0.00000	0.00000	0.00000
Offset Binary	1111 1111 1111 1111	−1.99950	−1.99975	−1.99988	−1.99994
	1000 0000 0000 0000	0.00000	0.00000	0.00000	0.00000
	0000 0000 0000 0000	+2.00000	+2.00000	+2.00000	+2.00000
Two's Complement	0111 1111 1111 1111	−1.99950	−1.99975	−1.99988	−1.99994
	0000 0000 0000 0000	0.00000	0.00000	0.00000	0.00000
	1000 0000 0000 0000	+2.00000	+2.00000	+2.00000	+2.00000

*For Voltage Amplifier, V_{OUT} is defined by Selected Feedback Resistor, R_{FB}: $V_{OUT} = -I_{OUT} \times R_{FB}$.
**For lesser bits, delete less significant bits.

ADJUSTMENTS

Built-in potentiometers may be adjusted to customize the MP19XXA Series of D/A Converters to system applications requiring trimming of Range (Gain) and/or Offset (Zero). The RANGE and OFFSET potentiometers are identified and located on the label, and access to them is made at the top of the Modupac.

To trim any offsets to zero, apply the coded input for zero signal, and trim OFFSET for a zero analog current or voltage output.

To adjust the range, apply a full-scale coded input and trim RANGE for the correct analog current or voltage output.

ORDERING GUIDE

Simply Specify

For	Enter
13-Bit Modupac™	MP1913A
14-Bit Modupac™	MP1914A
15-Bit Modupac™	MP1915A
16-Bit Modupac™	MP1916A
XX-Bit Card-Mounted MP	AN19XX

Output Voltage (AN Card-Mounted MP Only)

For	Enter
0 to +10V	1
±10V	2
±5V	3
0 to +5V	4

Input Code (AN Card-Mounted MP Only)

For	Enter
Binary, Offset Binary	A
*2's Complement — AN version only	D

Ordering Example: AN1915-A is a 15-bit card-mounted Modupac™ with a 0 to +10V output and binary input code.

*NOTE: To configure MP version for a 2's complement input, MSB must be inverted. When ordering AN types, inversion is included on P.C. card.

AN19XXA PIN CONNECTIONS

	1	A	INT REF
UPDATE	2	B	HOLD TRIG
B16	3	C	
B15	4	D	
B14	5	E	
B13	6	F	
B12	7	G	
B11	8	H	
B10	9	K	
B9	10	L	
+5V	11	M	B8
DIG RTN	12	N	
B7	13	P	
B6	14	R	
B5	15	S	
B4	16	T	
B3	17	U	
B2	18	V	
ANA RTN	19	W	OUTPUT RTN
−15V	20	X	FEEDBACK
+15V	21	Y	B1
OUTPUT	22	Z	OUTPUT

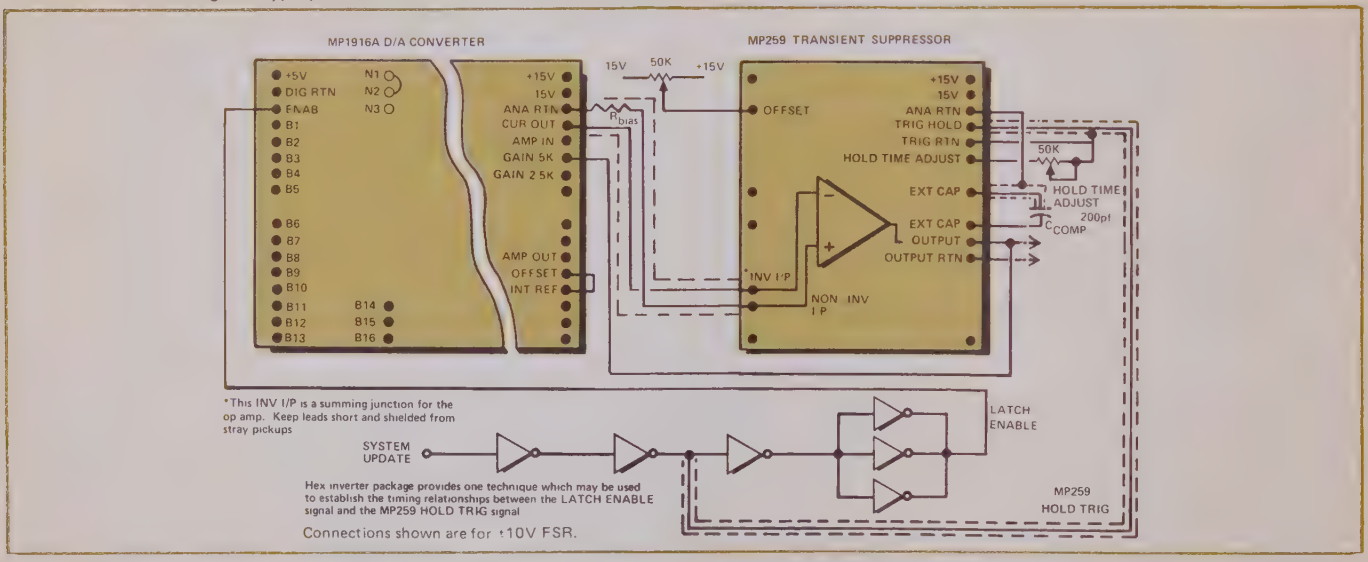


Figure 6. Simplified Schematic of MP1916A and MP259 Connected as Deglitcher with Added External Components

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Tel. (41) 1-810-0666 ■ Telex 845-59699
ANALOGIC LIMITED ■ 68 High Street ■ Weybridge, Surrey KT13 8BN ■ England
Tel. (44) 932-41251 ■ Telex 851-928030
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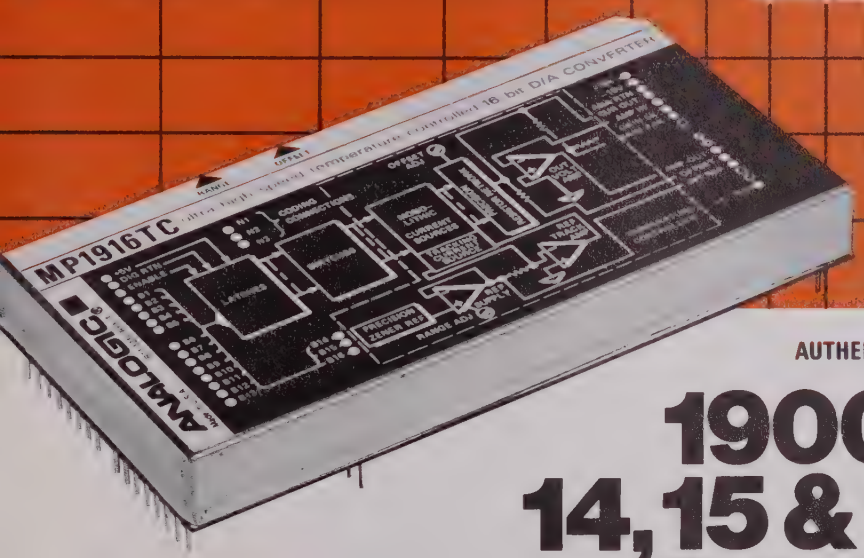


AUTHENTIC 16-BIT RESOLUTION . . . <1 PART IN 65,536

1900TC Series 14, 15 & 16-Bit D/A Converters

Ultra-High Stability, Accuracy, Speed & Temperature Controlled to Better than 1PPM/° C - - - ALL DRIFT SOURCES!

ANALOGIC®
. . . The Digitizers

Ultra-Stable, High-Precision 14, 15 & 16-Bit D/A Converters Advance DAC Thermal Stability to Better Than 1 PPM/°C . . . TOTAL!

DESCRIPTION

The result of Analogic's expertise in precision converter creativity, the 1900TC Series DACs provide the digital systems user with:

- Extremely high conversion speeds
- Superior linearity and absolute accuracy
- **Outstanding thermal stability**
- Versatile interface compatibility

These innovative converters offer 14, 15, and 16 binary-bit resolution at fast settling times to overcome the most exacting industrial and instrument D/A applications where the following requirements are mandatory:

- Precise data handling . . . essentially error free!
- Excellent reliability
- **Steadfast temperature control**
- Competitive cost

Ready for use as received and completely self-contained within a compact, fully-shielded case, the 1900TC Series includes the following BUILT-IN components:

- Storage registers
- Monolithic current switches
- Matched precision resistors
- Ultra-stable zener reference
- Gain and offset potentiometers
- Output voltage amplifier
- **Thermistor-sensing temperature controller**

• CONFIGURATION

The 1900TC Series converters can be plugged into a 44-pin connector (AN card-mounted module) or can be soldered to a PC card (MP module). Since the location of the gold-plated pins is standardized, direct interchangeability applies to all three converters in this series.

Advanced EMI and RFI shielding techniques assure stable operation within noisy electrical environments and allow unlimited physical positioning in any user's system or OEM building block application without generating mutual interference problems.

Thoroughly factory tested to ensure rated conformance to established specifications, each 1900TC Series converter is shipped with its own QC-acceptance certificate . . . an incontrovertible record of the converter's complete test and calibration history.

• THE ANALOGIC SUPER-STABLE DACs

For the ultimate in 16-bit resolution with all tempco's typically less than 0.25ppm/°C, send for brochure describing Analogic's state-of-the-art breakthrough design . . . the MP8116 D/A Converter. If the exceptional temperature stability of the 1900TC Series is not required, send for data sheet describing Analogic's 1900A Series D/A Converters.

PERFORMANCE MILESTONES

For incorporation into a multitude of wide dynamic range display and control systems, such as precision vector displays, automated semiconductor testers, automatic typesetters, frequency synthesizers, and nuclear reactor controls, the 1900TC Series delivers the following unprecedented performance:

Valid 14, 15, & 16 Bit Resolutions

- Guaranteed Monotonicity to 16 Bits over Full Temperature Span
- Exhaustive Error-Budget Analysis for Minimal Deviations
- Custom-Calibrated QC-Certified Test Data Sheet Supplied

Superb Accuracy

- Linearity within 0.001% FSR
- Absolute Accuracy within 0.002% FSR (Traceable to NBS)

Exceptional Thermal Stability

- High-Gain, Proportional Temperature Controller
- Better than 1ppm/°C . . . ALL DRIFT SOURCES! . . . Including TC's of Gain, Offset, Reference, and Differential Linearity . . . Over Any Specified 20°C Span between 0°C and +60°C
- Power Supply Sensitivity of 5ppm FSR/1% Change in DC Voltage

Very-High Conversion Speeds

- Settling Times of 1 to 3μs to 1 LSB for Full-Scale Step in Current Mode
- Settling Times of 5 to 10μs to 1 LSB for Full-Scale Step in Voltage Mode with Internal Amplifier

Versatile Interface Flexibility

- DTL/TTL Compatibility with Positive True Logic
- Output Voltages of ±10V, ±5V, 0 to +5V, or 0 to +10V
- Output Currents of ±2mA Bipolar or 0 to −4mA Unipolar
- Unipolar Binary, Offset Binary, or 2's Complement Digital Input Codes
- Powered by Standard ±15V and +5V Supplies
- Output Short-Circuit Protected

Virtually Noise-Free

- RFI and EMI shielded
- Isolated Digital and Analog Grounds
- Noise Level of 0.0008% FSR from DC to 1MHz

All-Inclusive Construction

- Rugged, Low-Profile, Metal Enclosure
- Direct Pin-Compatible Interchangeability for Entire Series
- Choice of Modupac™ Module or PC Card-Mounted Module
- Optimum Performance/Price Ratio

1900TC SERIES SPECIFICATIONS

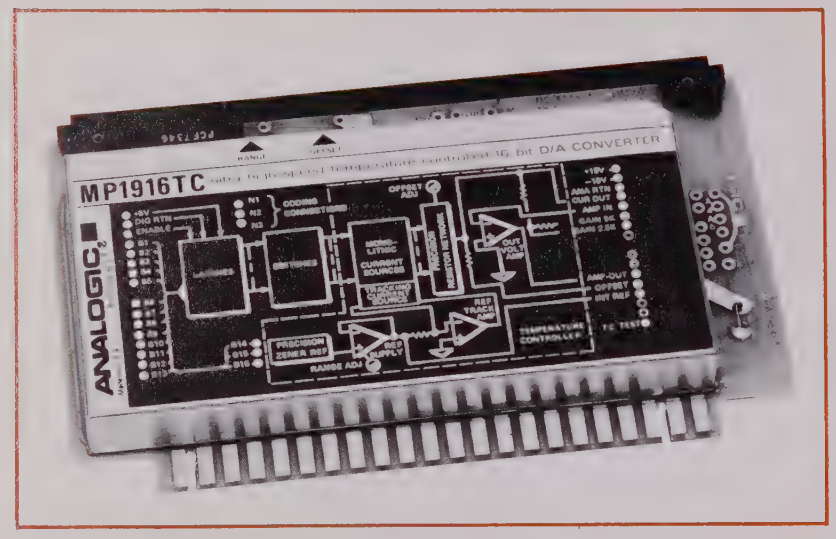
PARAMETER	MP1916TC	MP1915TC	MP1914TC
ANALOG OUTPUT			
Current Mode			
Full Scale Range	−2mA to +2mA, bipolar 0 to −4mA, unipolar	−2mA to +2mA, bipolar 0 to −4mA, unipolar	−2mA to +2mA, bipolar 0 to −4mA, unipolar
Impedance	1.25kΩ, bipolar 2kΩ, unipolar	1.25kΩ, bipolar 2kΩ, unipolar	1.25kΩ, bipolar 2kΩ, unipolar
Voltage Compliance	±1V maximum	±1V maximum	±1V maximum
Voltage Mode			
Full Scale Range	±10V, ±5V, 0 to +10V, 0 to +5V (pin selectable)	±10V, ±5V, 0 to +10V, 0 to +5V (pin selectable)	±10V, ±5V, 0 to +10V, 0 to +5V (pin selectable)
Impedance	<0.1Ω @ dc	<0.1Ω @ dc	<0.1Ω @ dc
Load Current	±5mA max. (includes feedback current)	±5mA max. (includes feedback current)	±5mA max. (includes feedback current)
DIGITAL INPUT			
DTL/TTL Compatible	2 loads	2 loads	2 loads
Number of Bits	16	15	14
Input Codes	Binary, 2's complement (pin selectable)	Binary, 2's complement (pin selectable)	Binary, 2's complement (pin selectable)
Enable	32 TTL Loads	32 TTL Loads	32 TTL Loads
INTERNAL REF. OUTPUT			
Voltage	6.5V ±0.15% (proportional to range control)	6.5V ±0.15% (proportional to range control)	6.5V ±0.15% (proportional to range control)
Output Impedance	<0.1Ω	<0.1Ω	<0.1Ω
Current Load	1mA maximum	1mA maximum	1mA maximum
SPEED			
Current Mode			
Settling Time to 1 LSB (Full Scale Step)	1μs typical 1.5μs maximum	.8μs typical 1.2μs maximum	.6μs typical 1.0μs maximum
Voltage Mode (Internal Amp)			
Settling Time to 1 LSB	10μs typ, 20μs max	10μs typ, 17μs max	10μs typ, 15μs max
Slew Rate	2V/μs	2V/μs	2V/μs
ACCURACY (@ +15°C to +35°C)			
Relative Accuracy (Linearity)	0.001% FSR	0.0015% FSR	0.003% FSR
Absolute Accuracy (NBS Traceability)	0.002% FSR	0.004% FSR	0.006% FSR
STABILITY (@ +15°C to +35°C)			
Current and Voltage Modes			
Total Combined Tempco's of Reference, Linearity, Gain and Offset	1ppm/°C maximum	1ppm/°C maximum	1ppm/°C maximum
For 0 to +15°C and +35°C to +60°C without Temperature Control	5ppm/°C maximum	5ppm/°C maximum	5ppm/°C maximum
Power Supply Sensitivity	5ppm FS/% change in dc voltage	5ppm FS/% change in dc voltage	5ppm FS/% change in dc voltage
POWER SUPPLY			
+15 ±0.5Vdc	DAC: 35mA typical plus load current Temperature Controller: 150mA initial, 60mA typical after warmup @ 25°C		
−15 ±0.5Vdc	35mA typical plus load current		
+5 ±0.25Vdc	180mA typical		
ENVIRONMENTAL & PHYSICAL			
Controlled Operating Temperature Range[2]	+15°C to +35°C	+15°C to +35°C	+15°C to +35°C
Storage Temperature Range	−25°C to +85°C	−25°C to +85°C	−25°C to +85°C
Relative Humidity	5% to 95%, noncondensing	5% to 95%, noncondensing	5% to 95%, noncondensing
Warmup Time	10 min. to spec. accuracy	10 min. to spec. accuracy	10 min. to spec. accuracy
Fault Protection	Output may be shorted to ground indefinitely without damage	Output may be shorted to ground indefinitely without damage	Output may be shorted to ground indefinitely without damage
Dimensions	4" W x 2" D x 0.44" H (101.6mm W x 50.8mm D x 11.2mm H)		
Shielding	RFI 6 sides; EMI 5 sides		

[1] Stabilities and temperatures given are for a normally specified DAC operation of +15°C to +35°C. For other temperature ranges, data may be shifted accordingly. See Note 2.
[2] Any 20°C span between 0°C and +60°C may be user-specified.

PRINCIPLES OF OPERATION

As shown in Figure 1, binary data is loaded in parallel into the internal latches by a high logic level at the ENABLE input. The latched outputs of the eight more significant bits drive quad switches that steer precision current sources either to the CURRENT OUTPUT or to ground. Exact current values are determined by the binary-weighted, precision, thermally tracking resistor network. This network converts the precision internal reference voltage into 16 precision currents which are gated to the output by the current steering switches. The eight less significant bits are provided by a monolithic digital-to-analog converter.

The entire package described above plus the gain-setting resistors associated with the output voltage amplifier are enclosed in a proportional temperature controller which, in turn, includes a thermistor, an operational amplifier, and a heating element. Temperature determines the thermistor output. When the exterior temperature ambient drops, the thermistor resistance increases. This action causes an increased amplifier output that forces more current through the heating element. Conversely, when the exterior temperature rises, less current flows through the heating element. Thus, a constant temperature, well within 1°C, is maintained for an exterior 20°C ambient span. Wider temperature ranges or different ambient spans can be user selected. See your Analogic representative for details.



MP1916TC PC Card-Mounted Module

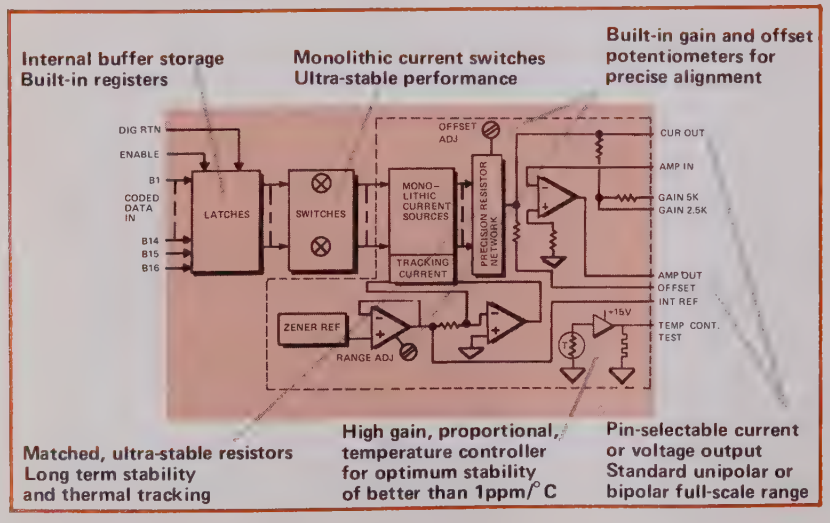


Figure 1. Functional Block Diagram of MP1916TC

TYPICAL APPLICATIONS

The 1900TC Series, a new class of precision converters, furnishes the mandatory stability, accuracy, and linearity needed for the following critical DAC applications: controlling beam energy in particle accelerators, positioning electron beams, and driving computer-controlled automatic-operating test equipment.

Nuclear Particle Deflection

In a high-energy research facility, an MP1916TC controls the deflection of an energy beam past a narrow aperture. Since deflection angle is proportional to particle energy, selection of only those particles of exactly the desired energy is achieved. Beam control stability (1ppm/°C) may be translated to miniscule deflection of the selected energy.

Electron Beam Positioning

Mask preparation for LSI devices by electron beam scribing is common industrial practice. This application requires exceptional performance in speed, accuracy (within 0.001mm), and repeatability. The 1900TC Series converters can be fully applied to these stringent requirements.

Computer-Driven Automatic Testing

Automatic testers demand a computer-programmable stimulus possessing crucial performance characteristics. The 1900TC Series offers 100,000 independent measurements per second (typical).

Other typical applications include: data distribution systems, industrial process controls, precision CRT displays, X–Y graphic plotters and recorders, machine tool numerical control systems, waveform synthesis and recovery, high resolution information translation systems, programmable control instrumentation and nuclear reactor controls.

ANALOGIC COMPATIBLE PRODUCTS

Analogic's highly effective MP259 Transient Suppressing Amplifier ("deglitcher") minimizes the transients resulting from the unavoidable glitches that occur at the switch outputs of D/A converters during major input code changes. Ideally suited for use with the 1900TC Series (see Figure 6), the MP259 can be connected to any high speed D/A converter for essentially "glitch-free" analog outputs. Send for MP259 application data.

Regulated dc power supplies, including line-powered and dc-to-dc converter modules, are manufactured by Analogic to furnish the standard +5 and ±15 voltages needed to operate the 1900TC Series converters, or any D/A or A/D converter. Line-powered modules include the MP3325 (+5V), the MP33315 (±15V), and the MP33515 (±5V and ±15V). The modular MP3020 converts +5Vdc into ±15Vdc. Send for the data sheets describing these specific modules or for a brochure covering the complete line of Analogic's regulated dc power supplies.

ACTION REQUEST

Analogic's Applications Staff is pleased to provide the following services to you:

Literature Available

- ☐ Please send "A Case for the 1900TC Series" – a compilation of technical articles and designer information.
- ☐ Please send your Short Form Catalog of Data Conversion Products.
- ☐ Please send data sheet(s) for the following product(s):

_____ _____

_____

Technical Assistance

☐ Please have a Senior Applications Engineer call to discuss

_____

_____

My product interest is:

- ☐ MP1914TC
- ☐ MP1915TC
- ☐ MP1916TC
- ☐ Other _____
- ☐ Card-Mounted AN19__TC
- ☐ MP8116
- ☐ Series 1900A

I am interested in D/A converters with substantially different characteristics:

- ☐ More resolution
- ☐ Higher speed
- ☐ Still higher stability
- ☐ Other _____
- ☐ Less resolution
- ☐ Lower speed
- ☐ Lower stability – lower cost

Related Products – I am interested in the following products:

- ☐ A/D Converters
- ☐ Sample & Hold Amplifiers
- ☐ DC/DC Converters
- ☐ Multiplexers
- ☐ Modular Power Supplies
- ☐ Transient Suppressor Amplifiers
- ☐ Total Data Acquisition System (please describe) _____

_____

_____

Other Products: _____

_____

Quotation Required:

Please quote the following products/quantity:

Model No.	1-9	10-24	25-49	50-99	100 or more
MP1914TC					
MP1915TC					
MP1916TC					
Card-Mounted AN19__TC					

My requirement is:

☐ Immediate ☐ 3-6 months ☐ For reference only

NAME _____

TITLE _____

COMPANY _____

ADDRESS _____

CITY _____ STATE _____ ZIP ____

PHONE ( ) _____ Ext. _____

Please fold and staple before mailing.

A CASE FOR THE 1900TC SERIES

Check off appropriate box on other side of this reply card to receive articles relating to conversion system design and interpretation of A/D/A converter specifications.

Noise Effects on Analog to Digital Conversion Accuracy

"A/D and D/A, Fact or Fancy?"

A/D and D/A Converters for High Speed Data Acquisition Applications

System Considerations Dictate A/D and D/A System Designs

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MP Configuration

The 1900TC 14- to 16-bit D/A Converters are factory equipped to permit users to select any of the standard performance options. These selections are accomplished by making appropriate connections externally at the module pins of the MP configuration.

Operation for binary, offset binary, or two's complement input code, voltage or current output mode, and the full-scale output range are determined by making the pin connections specified in Figure 2.

When using the current output mode, the built-in voltage amplifier is available for other system applications. However, if not used, the amplifier voltage output should be connected to AMP IN to prevent possible no-load amplifier oscillations from feedback coupling to the current output signal.

AN Configuration

Selection of performance options for the AN card-mounted configuration is made by connecting jumpers on the PC board. The converter output, whether operating in the voltage or current mode, appears at pins 22 and Z on the PC board connector, and is available for a feedback connection as shown in Figure 5. The necessary jumpers are identified in Figure 2 and are shown in Figure 5. Care should be taken to check the jumpers after installation.

OUTPUT AND CODING REQUIRED		JUMPERS	
		PIN JUMPERS ON MODULE	ADDITIONAL JUMPERS FOR AN VERSION
	0 TO 4mA		A4 TO J1
	−2mA TO +2mA	OFFSET (A12) TO INT REF (A13)	A4 TO J1
±10V	INTERNAL AMP	CUR OUT (A4) TO AMP IN (A5), GAIN 5K (A6) TO AMP OUT (A11), OFFSET (A12) TO INT REF (A13)	A11 TO J1
±10V	EXTERNAL AMP	CUR OUT (A4) TO (−IN*), GAIN 5K (A6) TO (O/P*) OFFSET (A12) TO INT REF (A13)	A4 TO J1 A6 TO J2
±5V	INTERNAL AMP	CUR OUT (A4) TO AMP IN (A5), GAIN 2.5K (A7) TO AMP OUT (A11), OFFSET (A12) TO TO INT REF (A13)	A11 TO J1
±5V	EXTERNAL AMP	CUR OUT (A4) TO (−IN*), GAIN 2.5K (A7) TO (O/P*), OFFSET (A12) TO INT REF (A13)	A4 TO J1 A7 TO J2
+10V	INTERNAL AMP	CUR OUT (A4) TO AMP IN (A5), GAIN 2.5K (A7) TO AMP OUT (A11)	A11 TO J1
+10V	EXTERNAL AMP	CUR OUT (A4) TO (−IN*) GAIN 2.5K (A7) TO (O/P*)	A4 TO J1 A7 TO J2
+5V	INTERNAL AMP	CUR OUT (A4) TO AMP IN (A5), GAIN 5K (A6) TO CUR OUT (A4)	A11 TO J1
+5V	EXTERNAL AMP	CUR OUT (A4) TO (−IN*) GAIN 2.5K (A7) TO (O/P*), GAIN 5K (A6) TO CUR OUT (A4)	A4 TO J1 A7 TO J2
UNIPOLAR BINARY OR OFFSET BINARY		N1 TO N2	N1 TO N2
TWO'S COMPLEMENT		N3 TO N2	N3 TO N2

NOTE The (+IN*) terminal of the external op amp should be connected to the ANA RTN Pin (A3) of the MP1916 via a resistor (1.2KΩ)
*Connection on external op amp. † See Figure 5

Figure 2. Mode and Full-Scale Range Jumper Connections

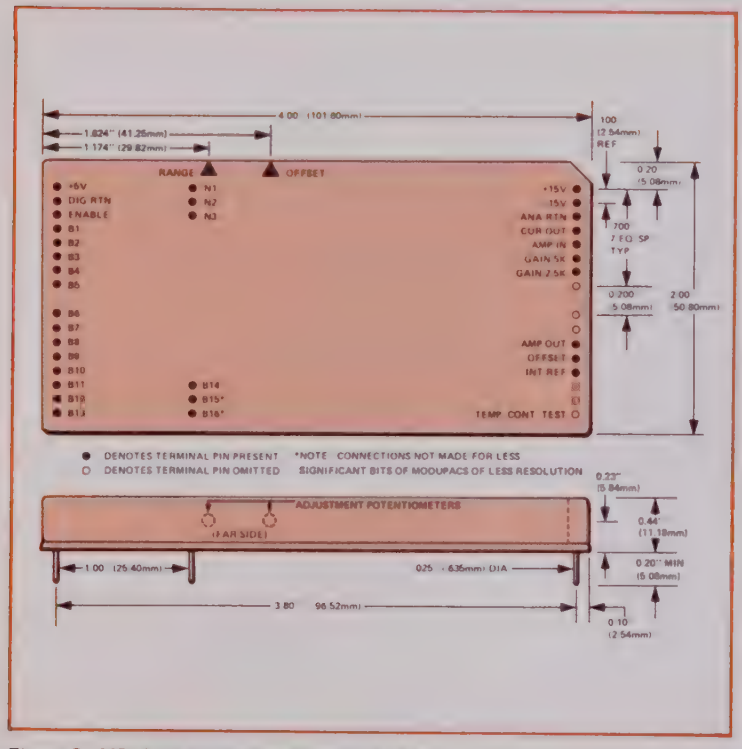

Figure 3. MP19XXTC Outline Drawing and Pin Locations

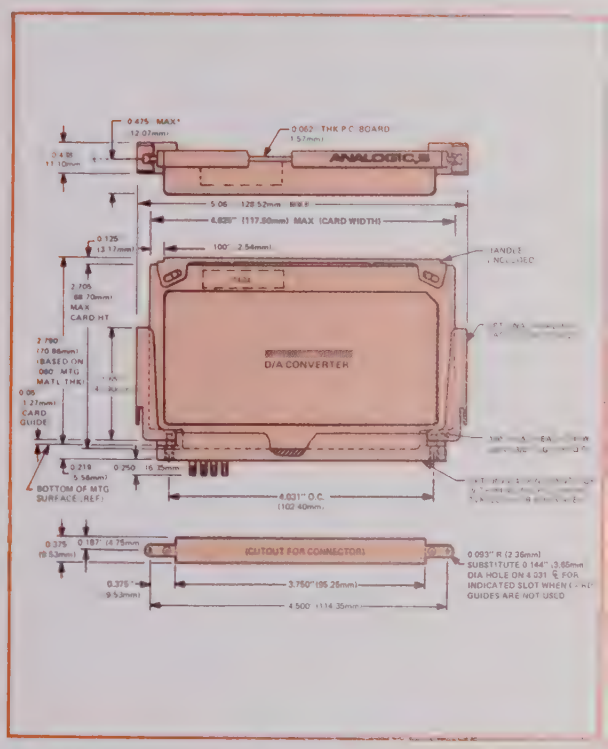

Figure 4. AN19XXTC Outline Drawing

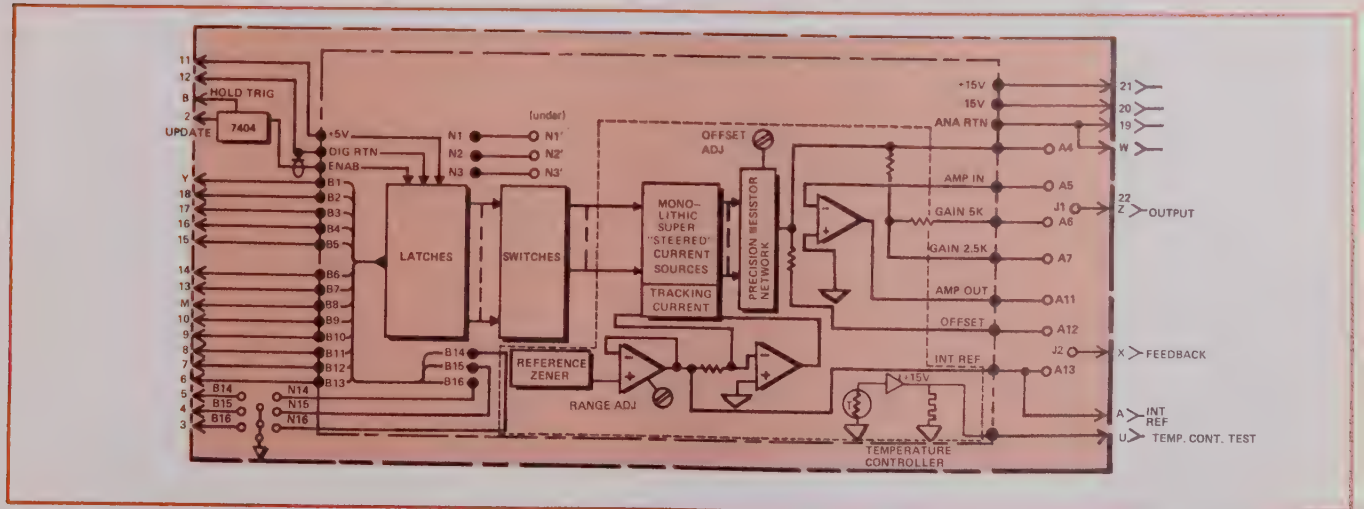

Figure 5. AN1916TC Jumper Terminals

DIGITAL INPUT DATA CODING				
FORMAT	INPUT CODE (MSB) (for 16 bits)**(LSB)	I_{OUT} Milliamperes* 1914TC	1915TC	1916TC
Unipolar Binary	1111 1111 1111 1111	−3.99975	−3.99988	−3.99994
	0000 0000 0000 0000	0.00000	0.00000	0.00000
Offset Binary	1111 1111 1111 1111	−1.99975	−1.99988	−1.99994
	1000 0000 0000 0000	0.00000	0.00000	0.00000
	0000 0000 0000 0000	+2.00000	+2.00000	+2.00000
Two's Complement	0111 1111 1111 1111	−1.99975	−1.99988	−1.99994
	0000 0000 0000 0000	0.00000	0.00000	0.00000
	1000 0000 0000 0000	+2.00000	+2.00000	+2.00000

*For Voltage Amplifier, V_{OUT} is defined by Selected Feedback Resistor, R_{FB}: $V_{OUT} = -I_{OUT} \times R_{FB}$.
**For fewer bits, delete less significant bits

ADJUSTMENTS

Built-in potentiometers may be adjusted to customize the MP19XXTC Series D/A Converters to system applications requiring trimming of Range (Gain) and/or Offset (Zero). The RANGE and OFFSET potentiometers are identified and located on the label, and access to them is made at the top of the Modupac.

To trim any offsets to zero, apply the coded input for zero signal, and trim OFFSET for a zero analog current or voltage output.

To adjust the range, apply a full-scale coded input, and trim RANGE for the correct analog current or voltage output.

ORDERING GUIDE

Simply Specify ——— [ ] — [ ] — [ ]

For	Enter
14-Bit Modupac™	MP1914TC
15-Bit Modupac™	MP1915TC
16-Bit Modupac™	MP1916TC
XX-Bit Card-Mounted MP	AN19XXTC

Output Voltage (AN Card-Mounted MP Only)

For	Enter
0 to +10V	1
±10V	2
±5V	3
0 to +5V	4

Input Code (AN Card-Mounted MP Only)

For	Enter
Binary, Offset Binary	A
*2's Complement	D

Ordering Example: AN1915TC-1-A is a 15-bit card-mounted Modupac™ with a 0 to +10V output and a binary input code.

*NOTE: To configure MP version for a 2's complement input, MSB must be inverted. When ordering AN types, inversion is included on P.C. card.

AN19XXTC PIN CONNECTIONS

	1	A	INT REF
UPDATE	2	B	HOLD TRIG
B16	3	C	
B15	4	D	
B14	5	E	
B13	6	F	
B12	7	H	
B11	8	J	
B10	9	K	
B9	10	L	
+5V	11	M	B8
DIG RTN	12	N	
B7	13	P	
B6	14	R	
B5	15	S	
B4	16	T	
B3	17	U	TEMP. CONT. TEST
B2	18	V	
ANA RTN	19	W	ANA RTN
−15V	20	X	FEEDBACK
+15V	21	Y	B1
OUTPUT	22	Z	OUTPUT

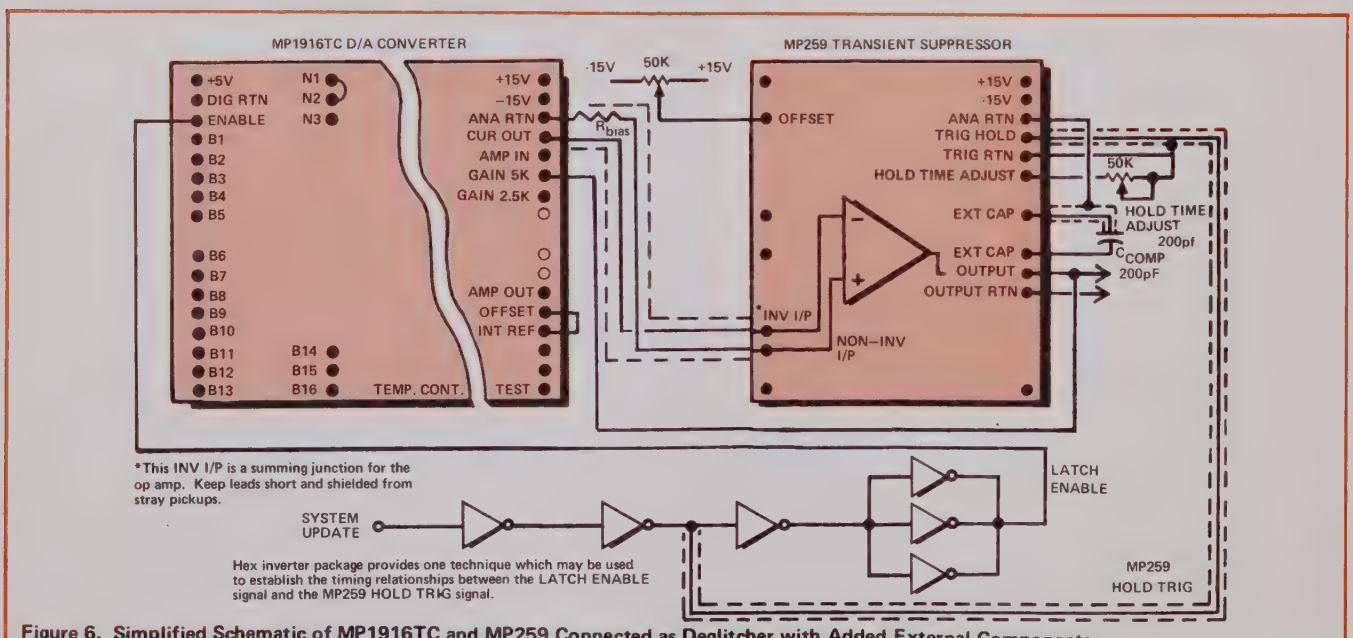

Figure 6. Simplified Schematic of MP1916TC and MP259 Connected as Deglitcher with Added External Components

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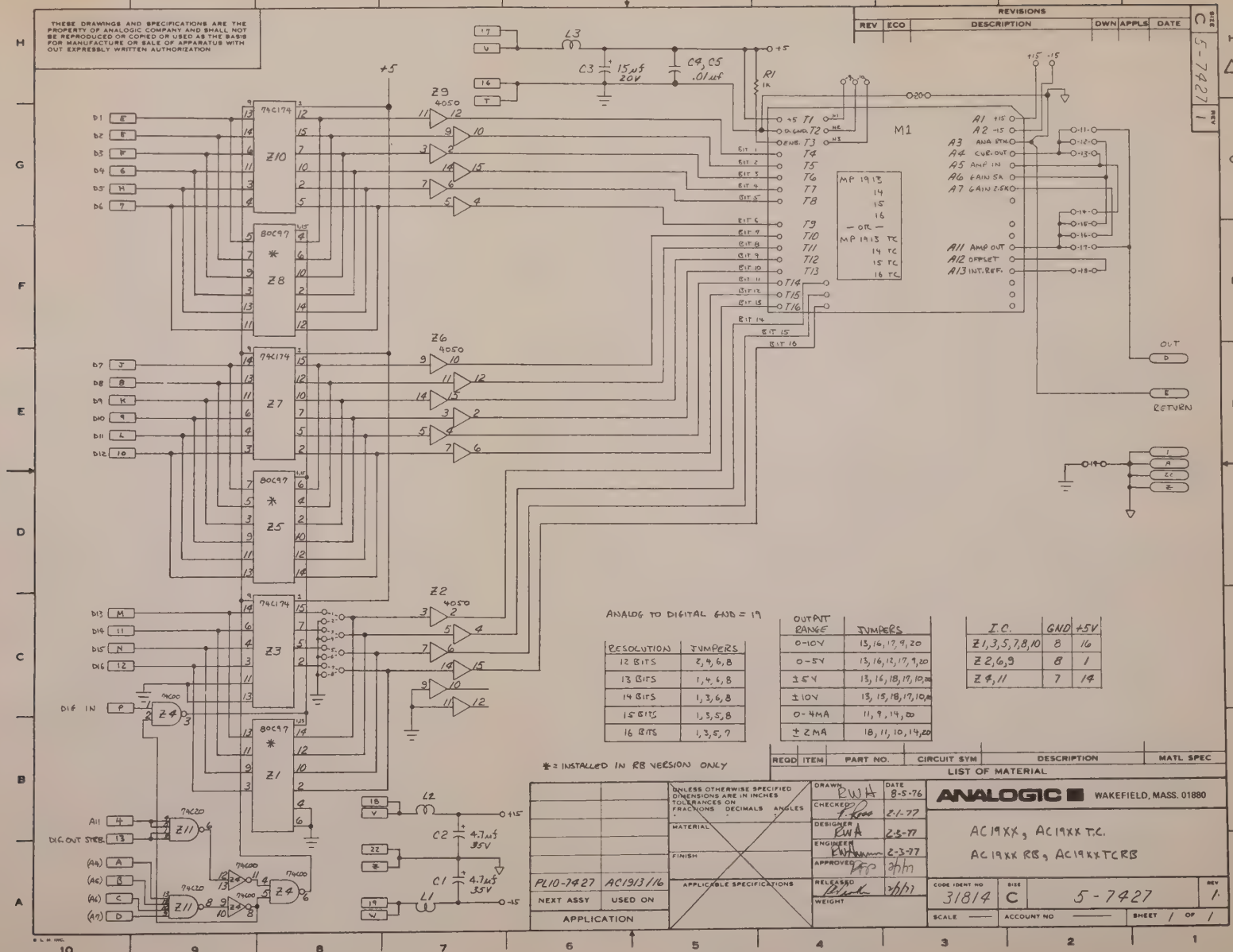
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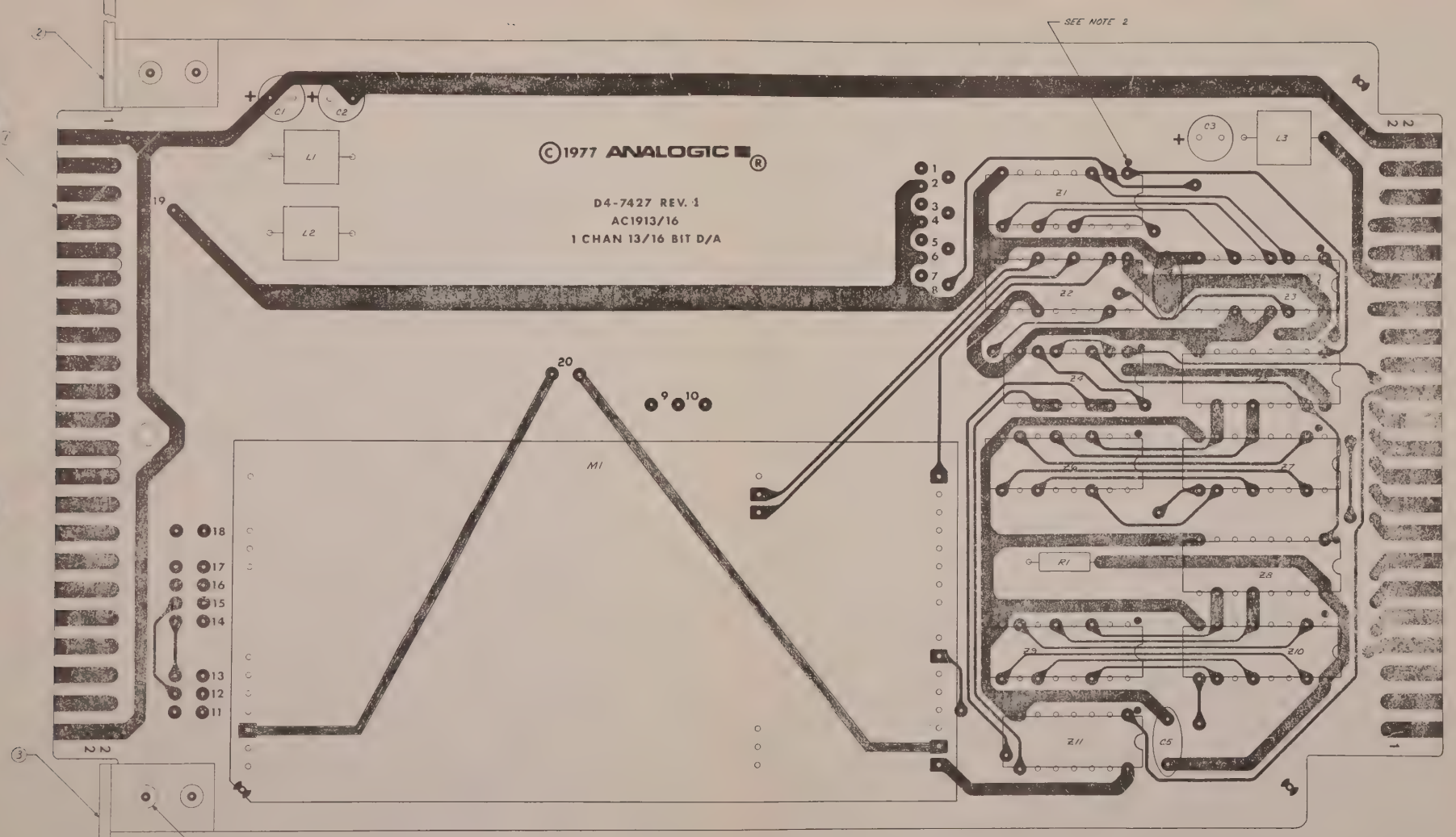
REVISIONS
REV | ECO | DESCRIPTION | DWN | APPLS | DATE
C 5-7427 1
+5
L3
C3 15µf 20V
C9, C5 .01µf
R1 1K
Z9 4050
Z10 74C174
Z8 80C97
Z7 74C174
Z6 4050
Z5 80C97
Z4 74C174
Z2 4050
Z3 74C174
Z1 80C97
M1
MP 1913
MP 1913 TC
OUT
RETURN
DIF IN
A11
DIG. OUT STRB.
L2
C2 4.7µf 35V
C1 4.7µf 35V
L1
+15
-15
ANALOG TO DIGITAL GND = 19
RESOLUTION | JUMPERS
12 BITS | 2,4,6,8
13 BITS | 1,4,6,8
14 BITS | 1,3,6,8
15 BITS | 1,3,5,8
16 BITS | 1,3,5,7
OUTPUT RANGE | JUMPERS
0-10V | 13,16,17,9,20
0-5V | 13,16,12,17,9,20
±5V | 13,16,18,17,10,20
±10V | 13,15,18,17,10,20
0-4MA | 11,9,14,20
±2MA | 18,11,10,14,20
I.C. | GND | +5V
Z1,3,5,7,8,10 | 8 | 16
Z2,6,9 | 8 | 1
Z4,11 | 7 | 14
* = INSTALLED IN RB VERSION ONLY
REQD | ITEM | PART NO. | CIRCUIT SYM | DESCRIPTION | MATL SPEC
LIST OF MATERIAL
PL10-7427 | AC19/13/16
NEXT ASSY | USED ON
APPLICATION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN RWA 8-5-76
CHECKED 2-1-77
DESIGNER RWA 2-3-77
ENGINEER 2-3-77
APPROVED
RELEASED
WEIGHT
ANALOGIC WAKEFIELD, MASS. 01880
AC19XX, AC19XX T.C.
AC19XX RB, AC19XX TCRB
CODE IDENT NO 31814
SIZE C
5-7427
REV 1
SCALE
ACCOUNT NO
SHEET 1 OF 1



NOTES:
1. FOR SCHEMATIC SEE C5-7427.
2. DOT INDICATES PIN 1 OF INTEGRATED CIRCUIT.
3. ASSEMBLE IN ACCORDANCE WITH A2-1027.

COMPONENT SIDE

REVISIONS			
DESCRIPTION	DWN	APPD'S	DATE

B. Ross	9-13-76	
J. A. Perkins	2-2-77	
[illegible]	2-3-77	
[illegible]	2-3-77	
[illegible]	2/11/77	
[illegible]	4/1/77	

PL10-7427 AC1913/16
APP. CATION

ANALOGIC [illegible] MASS.

ASSEMBLY
1 CHAN 13/16 BIT D/A
AC1913/16

31814 D 7-7427 1
1 OF 1

12
Digital Input

Card Number	Drawing Number	Title
DC6000/DC6100/DC6110	—	DC6000/DC6100/DC6110 Digital Input Module Data Sheet
DC6000/DC61XX	D5-7443	DC6000/DC61XX Digital Input Module Schematic
DC6000/DC61XX	D7-7443	DC6000/DC61XX Digital Input Module Assembly
DC62X0	—	DC62X0 32 Bit Change of State (COS) Card Data Sheet
—	—	Digital Input Interrupt Structure and Programming Examples
DC62X0	D5-8646	DC62X0 COS Card Schematic
DC62X0	D7-8646	DC620X COS Card Assembly
DC63XX	—	DC63XX Counter-Timer Card Data Sheet
DC63XX	D5-8645	DC63XX Frequency Counter Timer Schematic
DC63XX	D7-8645	DC63XX Frequency Counter Timer Assembly

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DC6000/DC6100/DC6110

DIGITAL INPUT FOR AN5400

GENERAL DESCRIPTION

The Analogic Model DC6000 and DC6100 are digital input cards featuring two (2) 16-bit parallel input ports, addressable and fully compatible with the AN5400 Data Acquisition System. The DC6100 has optically isolated inputs, while the DC6000 is nonisolated. Another isolated version, the DC6110 is available without input current determining resistors, allowing external control of drive current for increased speed.

Figure 1 is a simplified block diagram of the PCBs in this series, while Table 1 identifies the pin terminal assignments for each unit.

In the DC6100 and DC6110, the 32 inputs are arranged in blocks of 8, each block with its own VCC connection allowing isolation between inputs as well as between inputs and AN5400. See Figures 2 and 3. The input circuit configuration for each input to the DC6000 is shown in Figure 4.

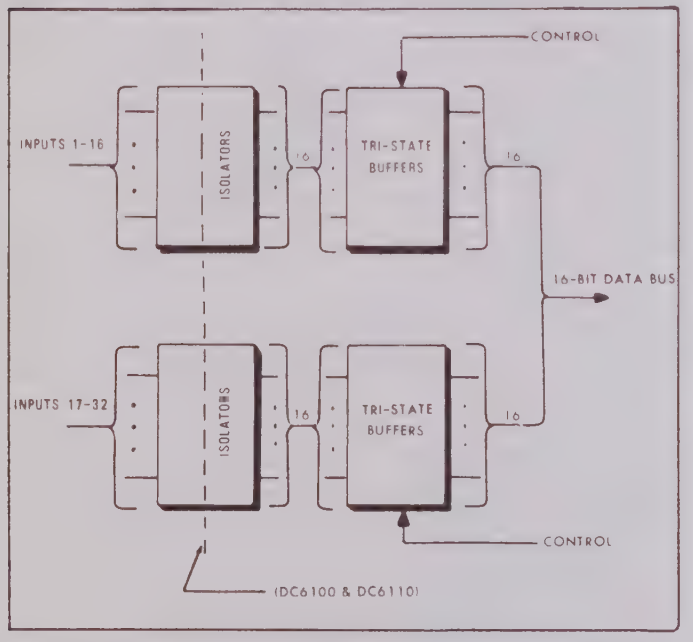

Figure 1. DC6000/DC6100/DC6600 simplified block diagram.

Specifications DC6000

Logical "0" Input Current (V_{IL} = 0 Volts)	1.6 mA MAX
Logical "I" Input Current (V_{IH} = 5 Volts)	1μA MAX
Propagation Delay (Worst Case)	160 nS MAX
Maximum Input Voltage	0≤ V_I≤ 5 Volts MAX
Threshold Level	2.5–3.5 VDC

Specifications DC6100, DC6110

Max Input Voltage (VCC-V_I)	0 to 32 Volts *
Max Input Current	15 mA
Logical "0" Input Current (VCC-V_I = 4.6 Volts)	1.6 mA *
Logical "I" Input Current (VCC-V_I = O)	0 mA
Breakdown Voltage (VCC to 5400 Chassis GND)	±500 VDC Min.
Breakdown Voltage (VCC to Any Other VCC)	±500 VDC Min
Capacitive Coupling (VCC to 5400 Chassis GND)	30 pF Max.
Propagation Delay (Worst Case)	50 μs
Threshold Current	0.1mA-1 mA

*DC6110 with 2K Input Resistor

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Table 1
User Pin Assignments for DC6XXX PCBs.

	VCC A	1	VCC
	17–24 B	2	1–8
(DC6000 ONLY)	DIG. GND --- C	3	--- DIG. GND (DC6000 ONLY)
(MSB)	17 --- D	4	--- 1 (MSB)
	18 --- E	5	--- 2
	19 --- F	6	--- 3
	20 --- H	7	--- 4
	21 --- J	8	--- 5
INPUTS	22 --- K	9	--- 6 INPUTS
	23 --- L	10	--- 7
	24 --- M	11	--- 8
	25 --- N	12	--- 9
	26 --- P	13	--- 10
	27 --- R	14	--- 11
	28 --- S	15	--- 12
	29 --- T	16	--- 13
	30 --- U	17	--- 14
	31 --- V	18	--- 15
(LSB)	32 --- W	19	--- 16 (LSB)
	X	20	
	VCC Y	21	VCC
	25–32 Z	22	9–16

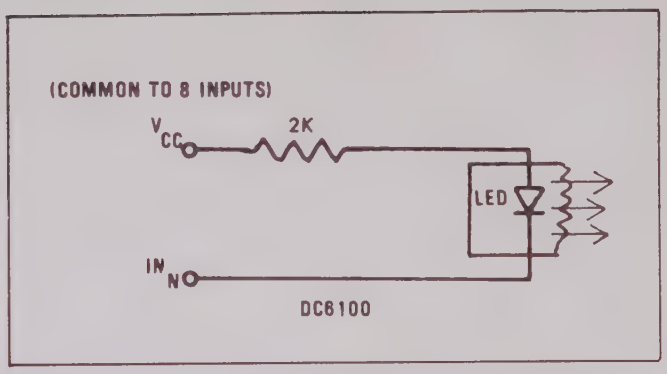

Figure 2. DC6100 optically isolated input configuration with current limiting resistor.

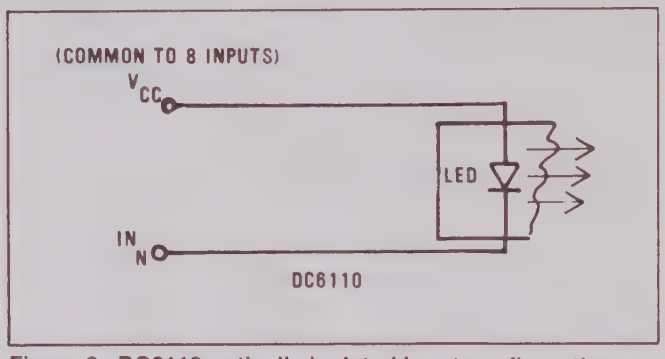

Figure 3. DC6110 optically isolated input configuration without current limiting resistor.

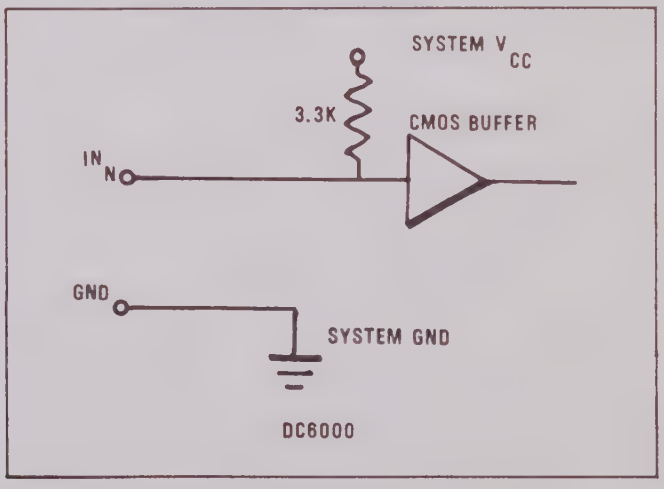

Figure 4. DC6000 input configuration, non-optically isolated.

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REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPR'D	DATE
0A	-	REDRAWN TO SHOW: ALL CIRCUITRY	J.L.	R.P.	12-6-77

PORT A

PORT B

ISOLATED VCC FOR INPUTS 1-8

ISOLATED VCC FOR INPUTS 9-16

DIG. GND (NONISOLATED VERSION)

ISOLATED VCC FOR INPUTS 17-24

ISOLATED VCC FOR INPUTS 25-32

21-232 HP 5082-4370

+5V

BOC97

74C10

LS4,10W

DIG. GND.

NOTES:

1. FOR DCL000 OMIT Z1-Z32 AND JUMPER PIN 3 TO 16. ADD JUMPER E1-E2. OMIT R1-R8, R17-R24, R33-R40 + R49-R56.
2. FOR DCL100 OMIT E1-E2, RETAIN Z1-Z32 AND R1-R8, R17-R24, R33-R40 + R49-R56.
3. FOR DCL110 OMIT E1-E2, R1-R8, R17-R24, R33-R40, AND R49-R56. ADD JUMPERS IN PLACE OF R1-R8, R17-R24, R33-R40 + R49-R56. RETAIN Z1-Z32.

R&D	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PL10-7443	DCL000 DCL1XX	
NEXT ASSY	USED ON	
APPLICATION		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON FRACTIONS ± DECIMALS ± ANGLES ±

MATERIAL

FINISH

APPLICABLE SPECIFICATIONS

WEIGHT

		DATE
DRAWN	L. J. MULLER	8-12-77
CHECKED	R. ROSS	1-19-77
DESIGNER	R. HAVENER	1-19-77
ENGINEER	R. HAVNER	1-19-77
APPROVED	R. F. FRANELLI	1-20-77
RELEASED	R. PEARCE	1-20-77

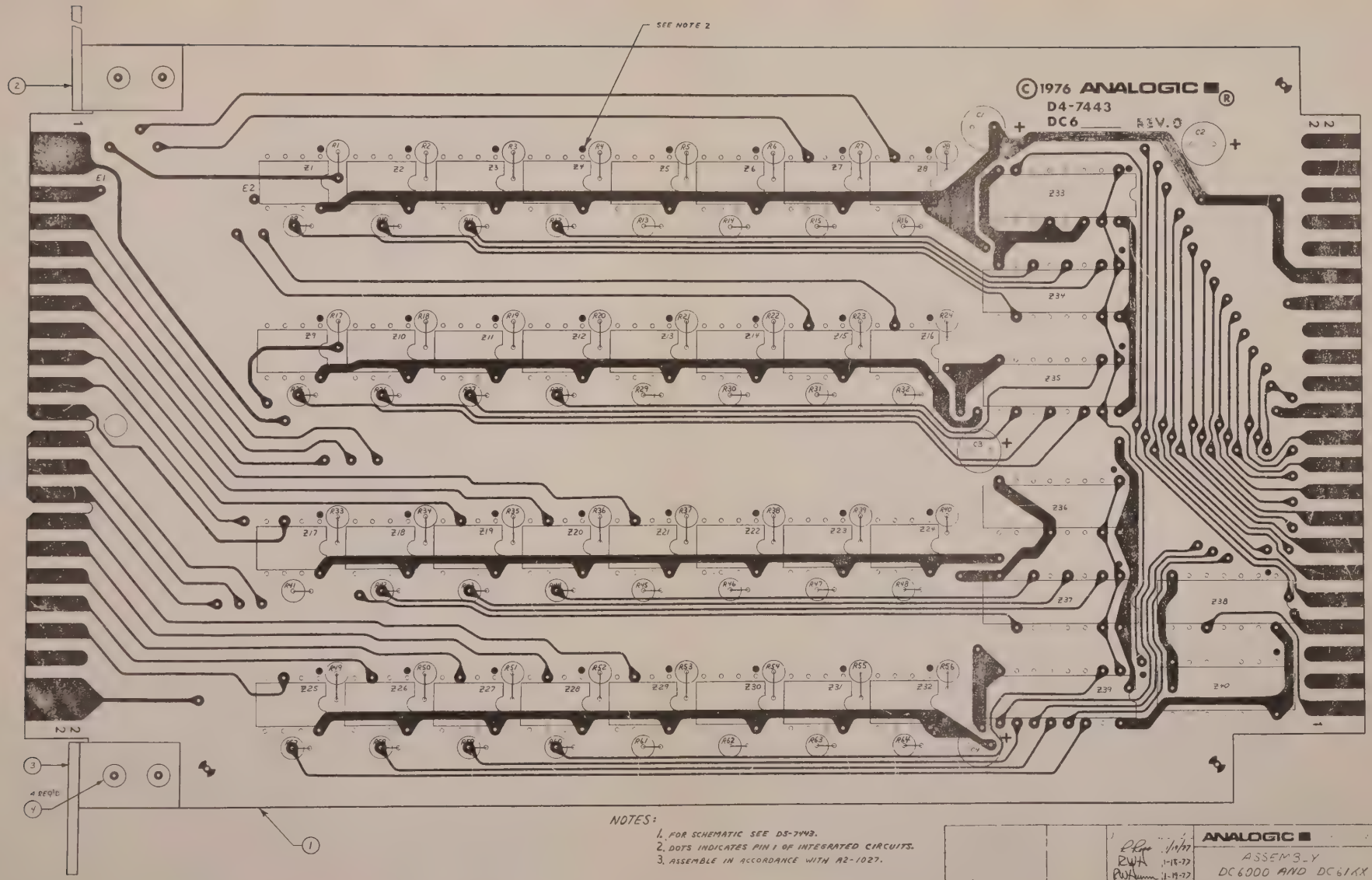
ANALOGIC WAKEFIELD, MASS. 01880

SCHEMATIC

DCL000 AND DCL1XX DIGITAL INPUT MODULE

CODE IDENT NO.	SIZE	DWG NO.	REV
31814	D	5-7443	0A

SCALE — ACCOUNT NO. — SHEET 1 OF 1


SEE NOTE 2
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D4-7443
DC6____ REV. 0
4 REQ'D
NOTES:
1. FOR SCHEMATIC SEE D5-7443.
2. DOTS INDICATES PIN 1 OF INTEGRATED CIRCUITS.
3. ASSEMBLE IN ACCORDANCE WITH A2-1027.
COMPONENT SIDE
ANALOGIC
ASSEMBLY
DC6000 AND DC61XX
DIGITAL INPUT MODULE
31814 D 7-7443

DC62X0

32-BIT CHANGE OF STATE CARD FOR ANDS5400

GENERAL DESCRIPTION

The Analogic Model DC62X0 is a 32-bit Change of State (COS) card which is organized in two 16-bit channels. It features TTL or optically isolated input with a vectored interrupt capability. The DC62X0 is fully compatible with the ANDS5400 Data Acquisition System. Each channel generates an independent interrupt whenever a change occurs in a 16-bit input word.

The DC62X0 COS card is available in two versions:
DC6200 2-channel, 16-bit COS card with TTL inputs.
DC6210 2-channel, 16-bit COS card with optically isolated inputs.

The user may select a unique vector for each DC62X0 via a 7-bit, PC-mounted switch. Upon interrupt, the ANDS5400 presents the vector to the CPU for appropriate action.

ELECTRICAL SPECIFICATIONS-DC6200

TTL Input

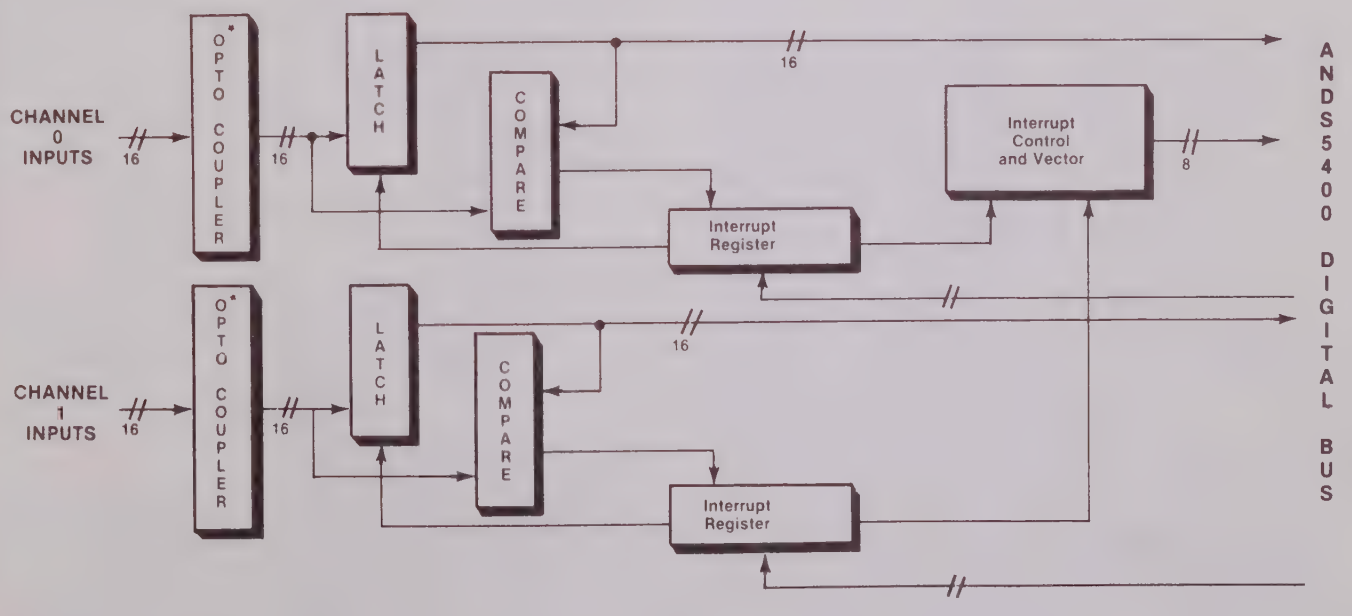
Low =	0.4Vdc max.
High =	2.0Vdc min.
Loading	1 unit load
Propagation Delay (Input Transition to Interrupt Request)	5μs max.

ELECTRICAL SPECIFICATIONS-DC6210[1]

Optically Isolated Input

Input Current Low	1.6mA max.
Input Current High	VCC ext. = 5Vdc. 0.3mA max.
Voltage Isolation	300Vac
Propagation Delay (Input Transition to Interrupt Request)	10μs max.

[1]VCC1, VCC2, VCC3, VCC4 are all mutually isolated. VCC1 supplies D1-D8 on Channel 0. VCC2 supplies D9-D16, Channel 0. VCC3 supplies D1-D8, Channel 1. VCC4 supplies D9-D16, Channel 1.



*DC6210 ONLY

Fig. 1. DC62X0 Functional Block Diagram

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FUNCTIONAL DESCRIPTION

A functional block diagram, indicating the major components of the DC62X0 COS card, is shown in Fig. 1. A 16-bit latch is provided in each channel to hold the current input word. A digital comparator checks for equality between the latch output and the card input. When an input change occurs, the comparator detects it, sets an interrupt request, and clocks the new data into the latch. The interrupt request is reset when the interrupt vector is read onto the ANDS5400 digital bus (see Fig. 4) by appropriate action of the host computer.

The speed at which changes may occur on individual bit inputs is determined by the rate at which the computer is able to service the interrupt. As noted above, the latch follows the input and is updated with each new change of state on any of its 16 inputs. Should two changes occur on any single bit, prior to interrupt service by the computer, the data representing the change on that bit will be lost.

Channel 0 always takes priority over Channel 1. Thus, if both channels should request an interrupt simultaneously, Channel 0 will apply its vector on the bus when the host computer calls for it. The two vectors are set by the PC switch, except for the LSB which is zero for Channel 0 and 1 for Channel 1 (see Fig. 4).

As shown in Fig. 1, each channel has its own Interrupt Register. These are Write Only registers used for enabling an interrupt in a given channel or for triggering an interrupt request (Test/Diagnostic). Data may be read through the COS card in a manner identical to that of a normal digital input card. At Power On, interrupts are initially disabled.

An external output is provided on the User connector from each channel which, when high, signifies that an interrupt is pending for that channel. This line is reset whenever the interrupt vector is read.

User pin connections are listed in Table 1.

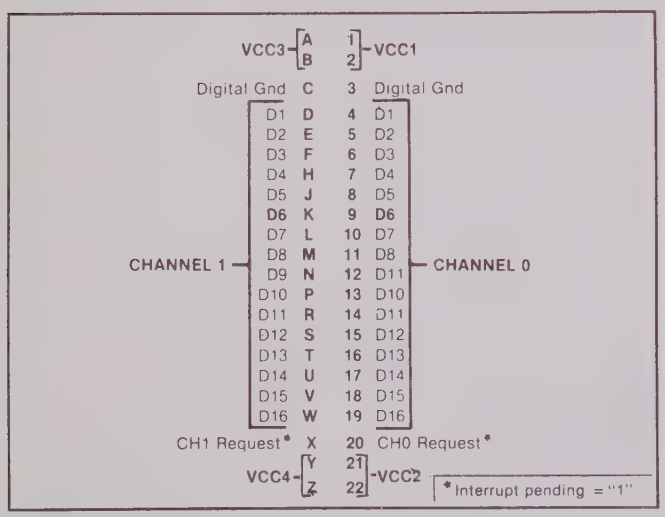

Table 1. User Pin Connections

ORDERING GUIDE

DC6200 — 2-channel 16-bit COS card TTL inputs.

DC6210 — 2-channel 16-bit COS card optically isolated inputs.

DC62X0 ADDRESSING

The address structure of the ANDS5400 provides complete flexibility of configuration and installation. Table 2 details the addresses of devices installed in a given enclosure. To determine the absolute address of this device, simply add the address indicated below to the enclosure address in the Digital Mode (See ANDS5400 Manual).

J1	0, 2	J9	40, 42
J2	4, 6	J10	44, 46
J3	10, 12	J11	50, 52
J4	14, 16	J12	54, 56
J5	20, 22	J13	60, 62
J6	24, 26	J14	64, 66
J7	30, 32	J15	70, 72
J8	34, 36	J16	74, 76

Note:
Addresses are R/W registers: Write for interrupt control; Read for data

Table 2. Relative Input Address Locations (Octal)

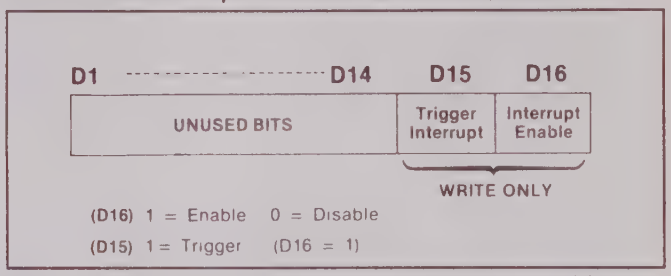

Fig. 2. DC62X0 Interrupt Control Register Data Field.

Fig. 3. Input Register Data Field.

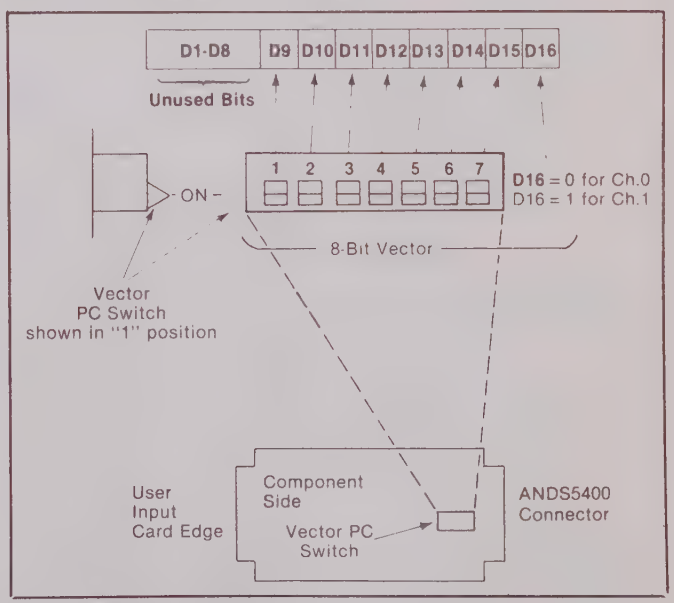

Fig. 4. DC62X0 Interrupt Vector.

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ANALOGIC AG ■ Kanalstrasse 15 ■ Postfach CH-8152 ■ Glattbrugg ■ Switzerland
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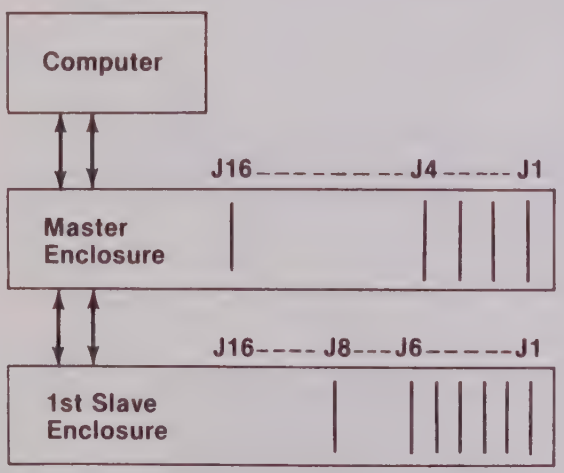
DIGITAL INPUT INTERRUPT STRUCTURE AND PROGRAMMING EXAMPLES

FOR ANDS5400

INTERRUPT STRUCTURE-HARDWARE

The hardware structure of the ANDS5400 extends interrupt capability to all user card slots within the system, thereby providing complete flexibility in configuration. The interrupt structure effectively implements parallel and daisy chain methods when seeking the interrupting device. This combination yields a fast and efficient method of determining the interrupting card (approximately 5μs for hardware to determine the interrupting device). The sequence of events, which determines the interrupting card, is described below.

During interrupt service, the master enclosure is tested for interrupt. If none is found, the second enclosure (1st slave) is tested and so forth to the last enclosure (7th slave). When the interrupting chassis is found, each card in the chassis is tested in sequence: Card slot 1 to Card slot 16. Using the above technique, the lowest number card slot in each enclosure has the highest priority in that enclosure, and the closer the enclosure electrically to the computer the higher its priority. Simply stated, the lower the address of the input card, the higher its priority.



Cards installed in J1 through J4 of the master chassis have the highest priority (J1 being the very highest priority slot). The Card at J16 may not be an interrupting device, since the daisy chain grant structure is broken. J1 of the first slave enclosure follows J4 of the master enclosure in priority. J6 is the lowest priority device shown. J8 cannot request interrupt service since the daisy chain grant structure is broken by vacant card slots.

Fig. 1. Interrupt Priority and Grant Structure.

The daisy chain must not be broken by vacant card slots within an enclosure since, under such conditions, interrupting devices "beyond" the vacant slot cannot request service. However, due to the structure of the interrupt hardware, vacant slots in "higher" priority chassis do not affect interrupt capability in "lower" priority chassis. (See Fig. 1.).

Each user card, capable of generating an interrupt, contains three fundamental elements (more elements may be present, depending on the type of card being used).

- An Interrupt Control Register — At a minimum, this register contains a read/write interrupt enable bit (1 = Enable) and an interrupt Trigger-bit (1 = Trigger) which, when written, simulates interrupt generation for testing and diagnostic purposes.

- A 6, 7, or 8-bit PC switch which, in conjunction with other hardware on the card, determines the interrupt vector; this is returned to the computer during interrupt servicing. (Only the lower 8 bits of the 16-bit digital input word contain meaningful information. The upper 8 bits are not used).

- A Digital Input Register which contains the data word.

The Interrupt Vector PC Switch, in combination with the general purpose nature of the ANDS5400, provides a useful method of improving the efficiency of interrupt handling routines. In most general purpose systems, the vector "looks up" the address of the interrupting device. However, in the ANDS5400, the vector can be used to report directly the address of the interrupting card, if appropriate care is taken when configuring the system. A maximum of 2^8 (256) interrupt vectors may be generated by user cards within the ANDS5400. In most cases, the interrupt generating cards may be configured into the first 256 digital addresses. By appropriately configuring the PC switches, the address of the data register can equal the vector and, therefore, may be used in the next step of the interrupt routine to gather the input data directly rather than executing a "look-up" subroutine.

When interrupts are enabled, requests can be generated at any time. During the period when a vector is read onto the bus, the priority chain is frozen. If a higher priority card interrupts during this period, its vector will not be read immediately but must wait until the next interrupt cycle.

INTERRUPT STRUCTURE-SOFTWARE

The normal sequence of events, which occur when handling an interrupt in the ANDS5400, is listed below (See Figure 2.). The interrupt service routine (software) is, of course, unique to the computer in use and, therefore, cannot be given in detail.

1. Interrupt request occurs from user card.
2. Interrupt request is asserted to host by ANDS5400 interface.
3. Host hardware determines whether or not to respond to interrupt. It will be assumed that host responds to the ANDS5400 interrupt.
4. ANDS5400 interface responds to interrupt acknowledge with an interrupt vector which, in turn, establishes the start address of the interrupt subroutine.
5. Host begins to execute subroutine.
6. The first ANDS5400 command in subroutine (other subroutine steps may precede first system command) is "Digital input at Address 4000".
7. The user card interrupt vector for the highest priority interrupt (other interrupts may have occurred within system during elapsed time) is placed on the ANDS5400 input bus (referred to computer). This vector may be used in a look-up table, as a function of the subroutine, or may represent the address of the register generating the interrupt. (See Interrupt Hardware Structure description preceding).
8. The host either "looks-up" appropriate register address or "turns around" card vector response (See Item 7).
9. The host asserts digital input at appropriate card address to ANDS5400 interface to service the interrupting card.
10. The subroutine performs action in response to data received from ANDS5400 input. This may involve further interaction with the ANDS5400 or other peripheral.
11. The host exits interrupt subroutine and handles other pending ANDS5400 interrupts (if any) by re-entering at Step 3 above.

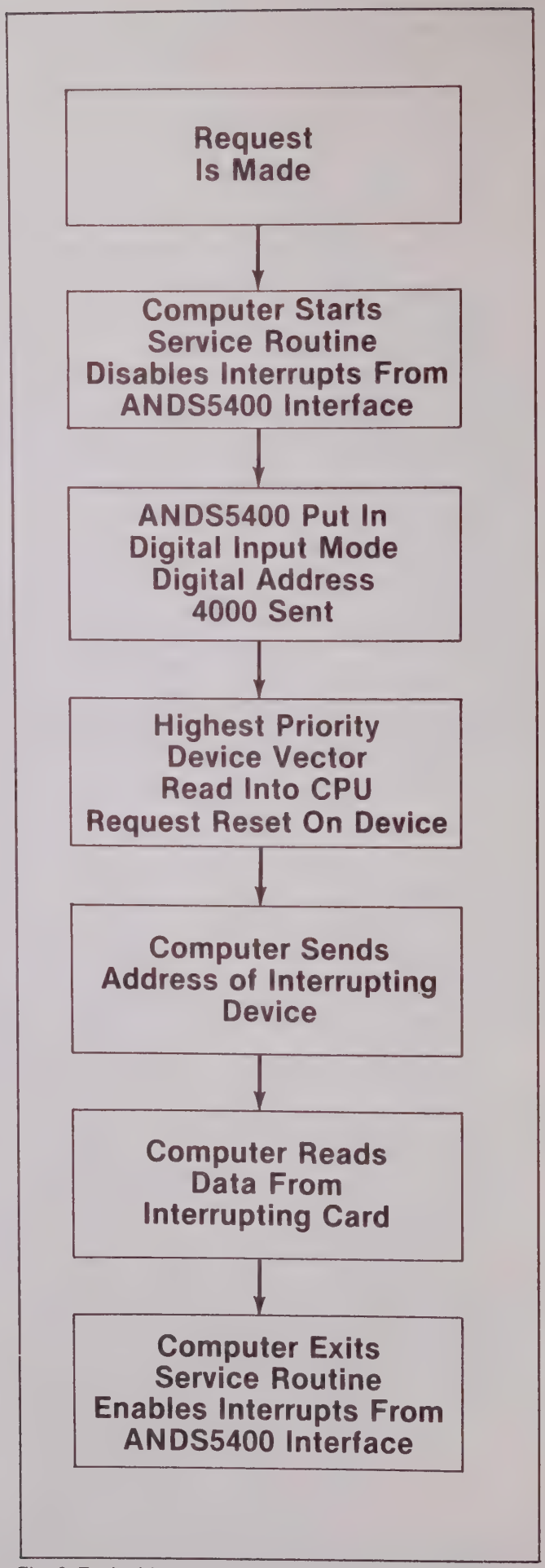

Request Is Made
Computer Starts Service Routine Disables Interrupts From ANDS5400 Interface
ANDS5400 Put In Digital Input Mode Digital Address 4000 Sent
Highest Priority Device Vector Read Into CPU Request Reset On Device
Computer Sends Address of Interrupting Device
Computer Reads Data From Interrupting Card
Computer Exits Service Routine Enables Interrupts From ANDS5400 Interface

Fig. 2. Typical Interrupt Service Sequence.

PROGRAMMING EXAMPLES — DC6300 COUNTER/TIMER INPUT/OUTPUT CARD

1. It is desired to measure the frequency of Input A, in Hz, without interrupts.

   - Address the Interrupt Register and load it with 000000_8. This disables interrupt.
   - Address the Time Base Register and load it with 000011_8. This sets mode and 1Hz gate time.
   - Address the Status Register and load it with 000001_8. This resets the counters and starts the gate.
   - Read back the Status Register and check bit D14. When it is zero, the gate is closed and counting is stopped.
   - Address the 16-bit Counter and read back frequency in Hz.

2. It is desired to measure the time period of Input B without interrupts, but using the read and reset feature of the DC6300.

   - Address the Interrupt Register and load it with 000000_8. This disables interrupt.
   - Address the Time Base Register and load it with 000074_8. This sets mode and time base to 1kHz.
   - Address the Status Register and load it with 000003_8. This sets Auto Reset mode and starts a measurement sequence.
   - Read back the Status Register and check bit D14. When it is zero, the gate is closed and counting is stopped.
   - Address the 16-bit Counter and read back the period of B in milliseconds.
   - Another counting sequence is now initiated automatically. Continue to read back the Status Register to check the gate (D14) and read back the Counter.

3. It is desired to count Input A to a preset number and then interrupt.

   - Address the Interrupt Register and load it with 000001_8. This enables interrupts.
   - Address the Time Base Register and load it with 000020_8. This sets mode.
   - Address the Status Register and load it with 000003_8. This resets the counters and enables Auto Reset mode.
   - Address the 16-bit Counter and load it with the 1's **complement** of the desired count (this also opens the gate).
   - At the end of counting, an interrupt will occur.
   - When the counter is read, or when preset again, another sequence (with interrupt) will begin.

PROGRAMMING EXAMPLES — DC6200 CHANGE OF STATE INPUT CARD

1. Read digital input when change of state occurs on input (Interrupt Enabled)

   - Address interrupt register and load it with 000001_8.
   - Address input register, read current value and store.
   - When change of state is sensed on input, interrupt will occur.
   - Address input register, read and compare to stored value.

2. The user desires to use the device as simply a static digital input (Interrupt Disabled).

   - Address interrupt register and load it with 000000_8.
   - Address and read input register when desired.

3. Test Interrupt Operation.

   - Address interrupt register and load it with 000003_8.
   - Interrupt should occur and return vector, as established by PC switch on the user card.

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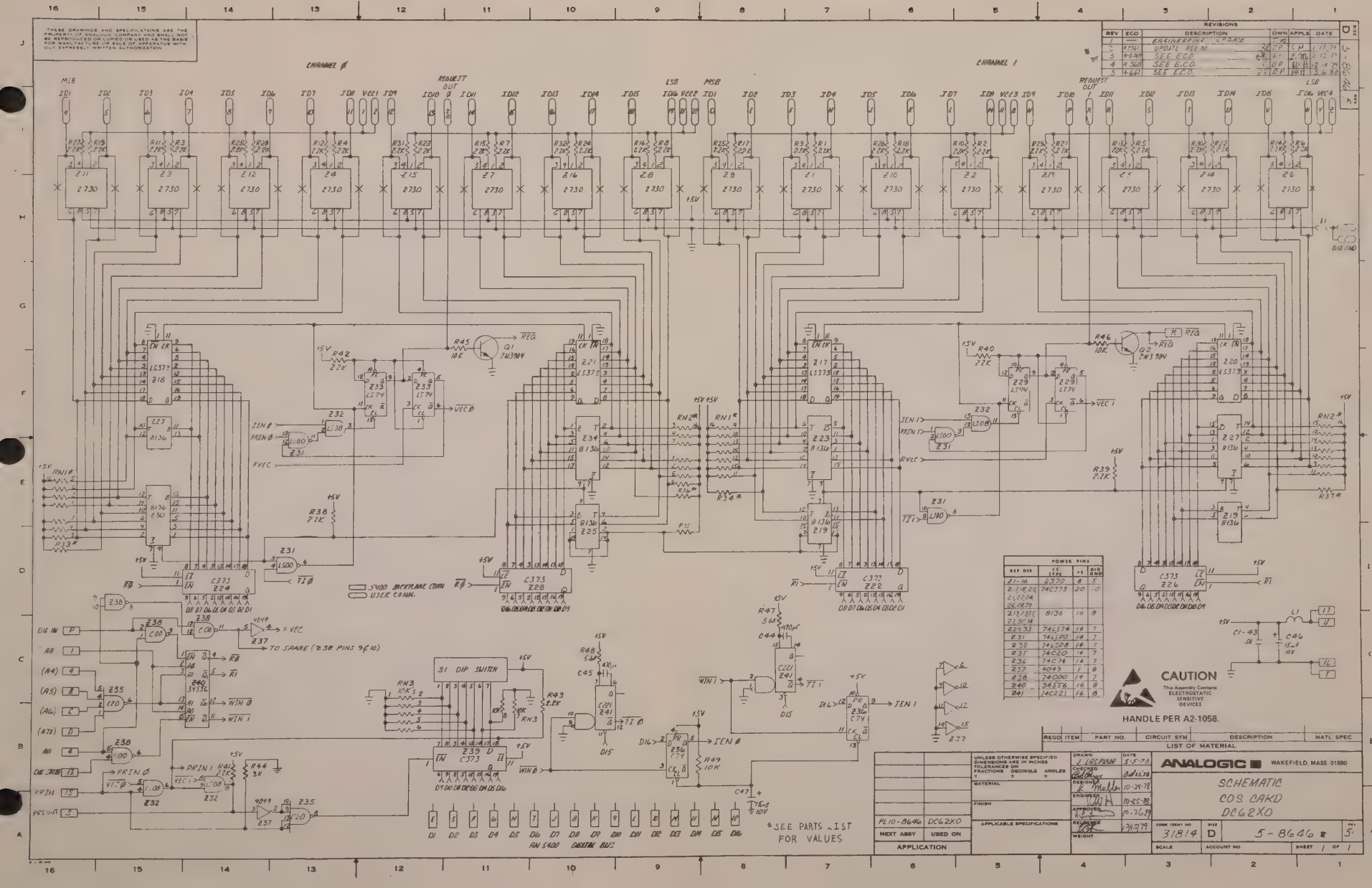

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REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
1	—	ENGINEERING RELEASE	JP		1-17-79
2	4-0341	UPDATE REPART	JP	LM	4-12-79
3	4-0349	SEE ECO	JP	LM	4-12-79
4	4-0368	SEE E.C.O.	JP	LM	4-19-79
5	4-0421	SEE E.C.O.	JP	LM	5-16-80

POWER PINS			
REF DES	IC TYPE	+5	DIG GND
Z1-16	2730	8	5
Z17,18,20, Z4,Z6,Z8, Z24,Z26,Z28	74C373	20	10
Z19,Z25	8136	16	8
Z29,33	74LS74	14	7
Z31	74LS00	14	7
Z32	74LS08	14	7
Z35	74C20	14	7
Z36	74C74	14	7
Z37	4049	1	8
Z38	74C000	14	7
Z40	34S36	16	8
Z41	74C221	16	8

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PL10-8646	DC62XO		
NEXT ASSY	USED ON		
APPLICATION			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON FRACTIONS DECIMALS ANGLES

MATERIAL

FINISH

APPLICABLE SPECIFICATIONS

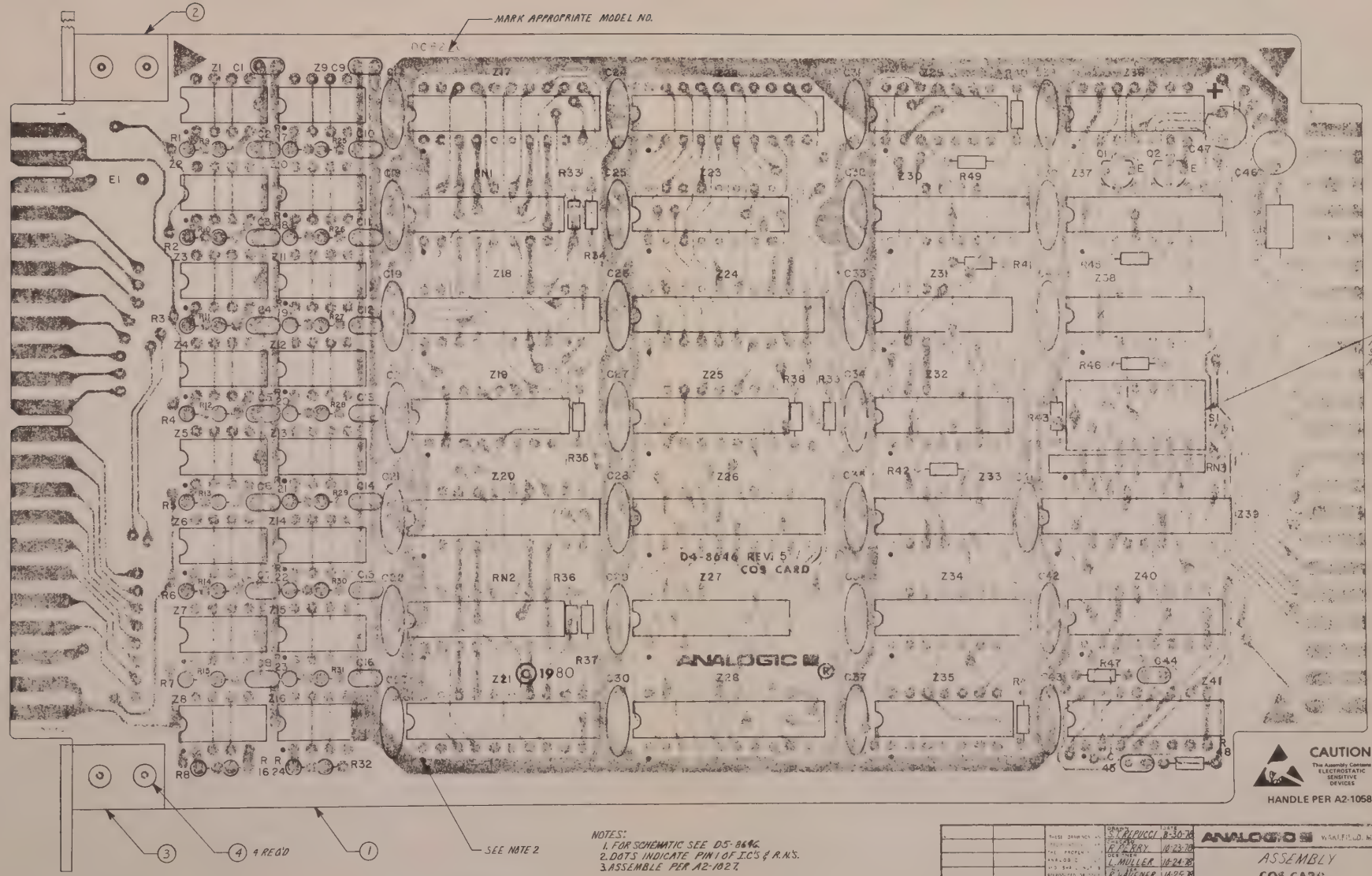
DRAWN	J. LOCKMAN	5-2-79
CHECKED		6/23/78
DESIGNED	L. Mullen	10-24-78
ENGINEER		10-25-78
APPROVED		10-26-78
RELEASED		2/6/79
WEIGHT		

ANALOGIC WAKEFIELD, MASS 01880

SCHEMATIC
COS CARD
DC62XO

CODE IDENT NO	SIZE	5-8646	REV
31814	D		5

SCALE | ACCOUNT NO | SHEET 1 OF 1



NOTES:
1. FOR SCHEMATIC SEE D5-8646.
2. DOTS INDICATE PIN 1 OF I.C.'S & R.N.'S.
3. ASSEMBLE PER A2-1027.

NO.	DESCRIPTION	DRWN	APPD'S	DATE
4	4568 SEE E.C.O.	CD	DR	DUE 12-14-79
5	4661 SEE E.C.O.	RC	DR	DUE 3-7-80

		DRAWN	R.PUCCI	8-30-78
		ENGR'G	R.C.BERRY	10-23-78
		QUAL ENGR	L.MULLER	10-24-78
		MFG ENGR	R.HAVENER	10-25-78
		APPROVED	M.CARNAVALE	10-26-79
PL10-8646	DC 62XO	MFG APPROVAL	K.MINBALL	10-15-79
NEXT ASSY	USED ON	WEIGHT		
APPLICATION				

ANALOGIC WAKEFIELD, MASS 01880

ASSEMBLY
COS CARD
DC 62XO

CODE IDENT NO	SIZE	DWG NO	REV
31814	D	7-8645	5

SCALE 4:1 | ACCOUNT NO | SHEET 1 OF 1

DC63XX

COUNTER-TIMER CARD FOR ANDS5400

GENERAL DESCRIPTION

The Analogic Model DC63XX Counter-Timer Card (CTC) is designed for accurate measurement of frequencies and time periods. This versatile card may also be used for simple event counting, frequency generation, and many other pulse accumulation/time base-related phenomena. The input to the computer from this card is the output of a 16-bit counter.

The DC63XX is fully compatible with the ANDS5400 Data Acquisition System, providing four basic modes of operation plus interrupt. For example, the CTC can count external events, up to a pre-programmed number, and can then interrupt the CPU. User connections are provided for special functions and cascading of a number of CTC's for higher resolution/counting. Optional signal conditioning is available for optically isolated and slow-moving analog input signals. Terminated input lines and relay contact closures can also be accommodated.

The DC63XX is available in five versions:

- DC6300 — TTL Input
- DC6301 — Optically Isolated Inputs
- DC6302 — Analog Inputs
- DC6310 — Expander Card
- DC6320 — Time Base Card

SPECIFICATIONS

Input Frequency

DC6300 — Input A to 10MHz
Input B to 1μs period.

DC6301 — Input A to 8MHz with >5mA drive
Input B to 1μs period with >5mA drive.

DC6302 — Inputs A, B to 1MHz with ±1V drive.

Logic Outputs

f_{out}	2 TTL Load Capability.
Counter Enable	2 TTL Load Capability.
Carry	2 TTL Load Capability.
Reset	2 TTL Load Capability.
External Input	1 TTL Load.
Carry, Count Input (Exp*)	1 Low power TTL load.
Reset Input	1 CMOS load.

*Expander card only.

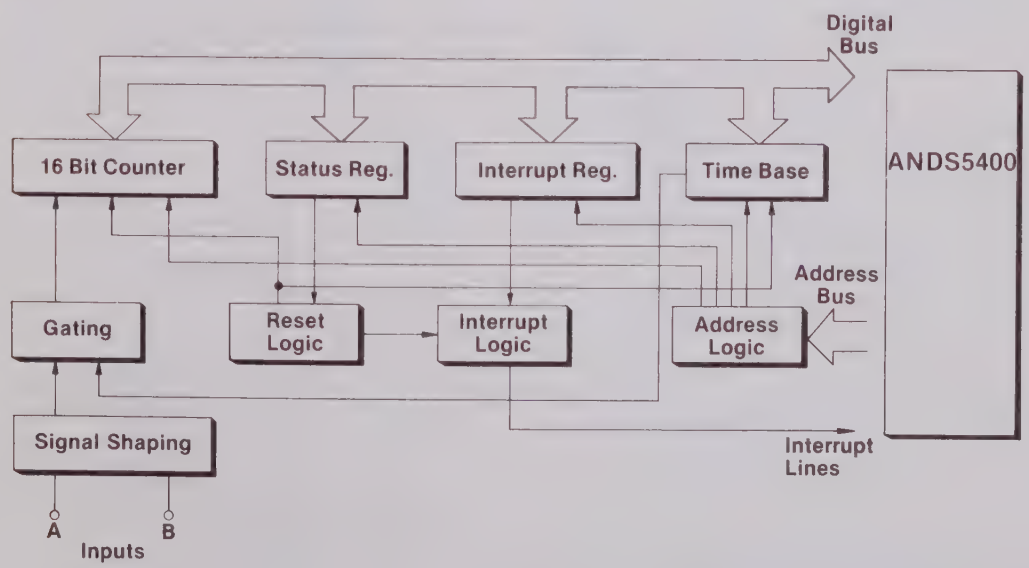


Figure 1. DC63XX Functional Block Diagram.

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FUNCTIONAL DESCRIPTION

A simplified functional block diagram, showing the DC63XX Counter-Timer Card (CTC) organization, is shown in Fig. 1. The card is comprised of four major components:

1. A 16-bit binary counter, that may be parallel-loaded and read using the ANDS5400 digital bus,
2. A timebase which may be parallel-loaded from the bus to set mode and output frequency,
3. A status register which provides a means of re-setting the counter and reading the state of the Done bit to determine the completion of a timing cycle, and
4. An interrupt register which provides 2 bits to enable interrupts or trigger an interrupt cycle.

The interrupt vector is determined by the PC switch, as shown in Fig. 12.

The signals at external inputs A and B undergo signal conditioning, determined by the particular version of the CTC being used, and are applied along with the Time Base output to gating logic. The method of gating is controlled by the user programmed mode.

Four basic functions and interrupt modes are available on the DC63XX Counter-Timer Card:

- Measure frequency of Input A with the Time Base as gate.
- Measure frequency of Input A with Input B as gate.
- Measure time period of Input B.
- Count Input A until a preset number is reached.

ADDRESSING

The address structure of the ANDS5400 provides complete flexibility of configuration and installation. The DC63XX CTC contains four registers as shown in Table 1. Each register has a read/write capability. The ANDS5400 must be in the digital output mode when communicating with a Write register and digital input mode when communicating with a Read register. Table 2 details the potential addresses of devices installed in any enclosure. To determine the absolute addresses of a DC63XX, simply add the enclosure address to the card addresses shown in Table 2 (see also the ANDS5400 Manual).

CTC Register	Address Bits		RELATIVE REGISTER ADDRESS
	A8	A9	Octal
16-Bit Counter	0	0	0
Time Base	0	1	1
Status Register	1	0	2
Interrupt Register	1	1	3

Table 1. Address of Card Registers.

J1	0, 1, 2, 3	J9	40, 41, 42, 43
J2	4, 5, 6, 7	J10	44, 45, 46, 47
J3	10, 11, 12, 13	J11	50, 51, 52, 53
J4	14, 15, 16, 17	J12	54, 55, 56, 57
J5	20, 21, 22, 23	J13	60, 61, 62, 63
J6	24, 25, 26, 27	J14	64, 65, 66, 67
J7	30, 31, 32, 33	J15	70, 71, 72, 73
J8	34, 35, 36, 37	J16	74, 75, 76, 77

Table 2. Address Locations (Octal) Digital Address Mode.

16-BIT BINARY COUNTER

The 16-bit counter provides two basic initialization states which may be controlled by the operator in local mode or by the computer when in the remote mode of operation. These are "clear" or count from (parallel loaded) preset. The counter output is read via the ANDS5400 digital bus and may be reset or cleared by the Read operation, if so programmed (refer to interrupt structure and programming examples in Section 8 of the Data Sheet Book and the Status Register Description herein). Fig. 2 details the counter word format.

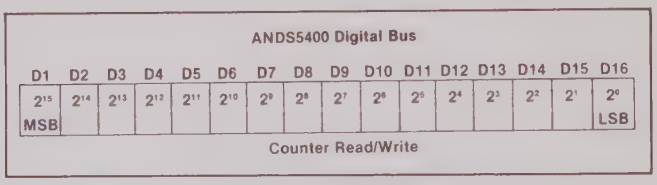

Fig. 2. Counter 16-Bit Input Word Format.

TIME BASE AND MODE CONTROL

The Time Base and Mode Control Register, shown in Fig. 3, determines the operating characteristics of the card. Utilizing the appropriate bit combinations, the user may program the device manually or under computer control to perform its widely varied functions. Table 3 lists the divisor bit pattern and resulting output frequency (f_{out}) if used in the internal oscillator mode. Should the user elect to input his own clock (up to 2MHz) the output frequency will vary accordingly.

(D13, D14, D15, D16) A through D — Output frequency (divisor) select (see Table 3).

(D10) Clock — 1 = External Oscillator
0 = Internal Oscillator

(External oscillator is a TTL waveform minimum 1μs pulse width, at a frequency $\leq$2MHz).

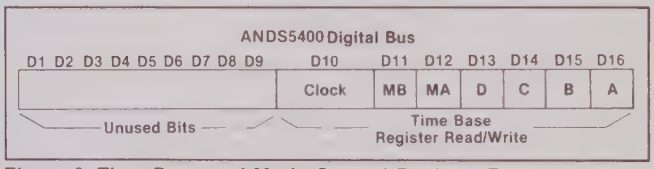
ANDS5400 Digital Bus
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16
Clock MB MA D C B A
Unused Bits
Time Base
Register Read/Write

Figure 3. Time Base and Mode Control Register Format.

Time Base Register				(÷) Divisor	*fout
D	C	B	A		
0	0	0	0	1	Ext. In.
0	0	0	1	2×10^4	50Hz
0	0	1	0	DO NOT USE	
0	0	1	1		
0	1	0	0	6×10^8	10 Min.
0	1	0	1	36×10^8	1 Hour
0	1	1	0	6×10^7	1 Min.
0	1	1	1	10^8	0.01Hz
1	0	0	0	10^7	0.1Hz
1	0	0	1	10^6	1Hz
1	0	1	0	10^5	10Hz
1	0	1	1	10^4	100Hz
1	1	0	0	10^3	1kHz
1	1	0	1	10^2	10kHz
1	1	1	0	10	100kHz
1	1	1	1	1	1MHz

*f_{out} when Internal 1MHz is used. (D10 = 0 in Time Base Register).
f_{out} (External Input) = f_{in}/Divisor

Table 3. Time Base Programming

OPERATING MODES

D11 = MB
D12 = MA — Mode Select — See Table 4.

Frequency Count Input A, Internal Gate MB = 0, MA = 0

This Mode connects Input A to the Counter input and the Time Base output to the Counter Enable input. If the Time Base is programmed for a 1-second gate time, the number in the Counter at the end of that time will equal the frequency of A in Hz. If interrupts are enabled, an interrupt will be generated. The counter is advanced on the **positive edge** of the signal.

Count Preset A **MB = 0, MA = 1**

This Mode connects Input A to the Counter input, and the Counter Enable input to the Carry output. If a number is preset into the Counter, the CTC will count Input A until a carry occurs; then it will stop and, if interrupts are enabled, an interrupt will be generated. The complement of the desired number of counts must be preset into the Counter. The Counter is advanced on the **positive** edge of the signal.

Frequency Count A, External Gate **MB = 1, MA = 0**

This Mode is the same as Mode Zero except that the Counter Enable is connected to Input B instead of the Time Base. The Gate period will be between **negative transitions** of Input B. If interrupts are enabled, an interrupt will be generated at the end of the counting period.

Time B **MB = 1, MA = 1**

This Mode connects the Time Base to the Counter input, and Input B to Counter Enable. If the Time Base is programmed for 1kHz, the Counter output will equal the time between **negative transitions** of Input B in milliseconds. If interrupts are enabled, an interrupt will be generated at the end of the timing sequence.

MB	MA	Mode	Description
0	0	0	Count A Internal Gate
0	1	1	Count Preset A
1	0	2	Count A External Gate
1	1	3	Time B

Table 4. Mode Selection.

STATUS REGISTER

The 3-bit Status Register controls resetting of the CTC and indicates the state of the Done bit. The Done bit is tested to determine if operation is complete when the interrupt is disabled. The 3-bit word is shown in Fig. 4.

(D16) 1 = Reset. When set, this bit resets the Counter to zero, resets the Time Base f_{out} line to a high level, and initiates one counting sequence. The reset pulse is available as a 10μsec positive pulse at the user edge connector (see Fig. 11).

(D15) 1 = Enable. This bit enables the Auto Reset feature of the CTC. This feature automatically resets the Counter and starts a new measurement sequence whenever the contents of the Counter are read onto the ANDS5400 bus.

(D14) 1 = count in progress 0 = counting completed. This is a Read Only bit that indicates when the CTC has completed a count sequence.

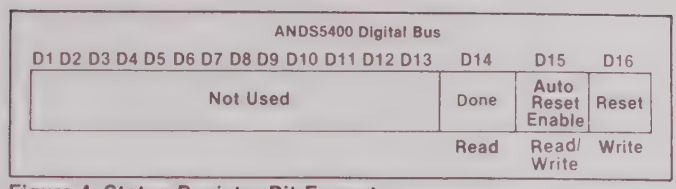

Figure 4. Status Register Bit Format.

INTERRUPT REGISTER

This 2-bit register is used for controlling CTC interrupts on the ANDS5400 bus. The register is detailed in Fig. 5.

(D16) Interrupt Enable — 1 = Enable. This bit controls interrupt generation on the CTC. When equal to zero, it prevents the card from asserting the request line and maintains the priority chain to lower priority cards. This bit is set to the zero state (disabled) during the system power up sequence.

(D15) Trigger Interrupt Request — 1 = Trigger. With D16 enabled, this bit generates an interrupt request from the card for testing purposes.

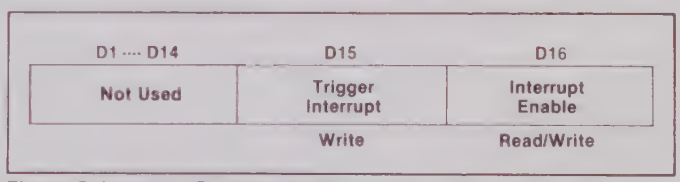

Figure 5. Interrupt Register Bit Format.

INPUT CONDITIONING

A wide variety of input conditioning permits the DC63XX to accept most types of input signals. Channels A and B may each have one of three types of signal conditioning. Input equivalent circuits are shown in the summaries below. Note that in all versions of this device, the Counter advances on the positive edge of the input and the Counter Enable changes state on the negative edge.

TTL DC6300

The DC6300 accepts TTL low power and low power Schottky inputs. Hysteresis is provided for greater noise immunity. Fig. 6 provides an input equivalent diagram for inputs AR and BR.

Should the user require terminated inputs, 50Ω for example, simply install 50Ω 10% carbon composition resistors (see Fig. 6) at R23 and R35 (near user edge connector pin 16).

Relay contacts may also be used to input the DC6300 for low speed counting applications. To implement the debounce circuitry, install jumpers E1 and E4 (near user edge connector pin 1). A Form C relay may then be used to input the DC6300, as shown in Fig. 7. Grounding $\overline{AR}$ or BR advances the Counter or changes the state of the Enable, respectively.

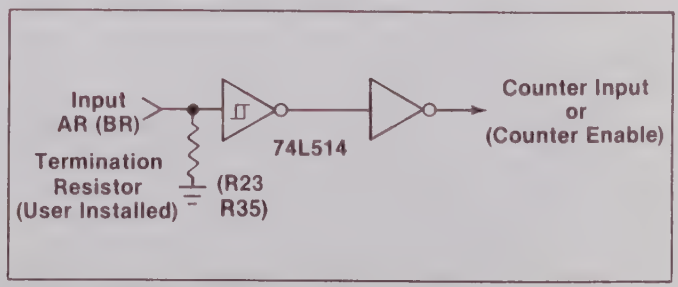

Figure 6. DC6300 TTL Input Equivalent Circuit.

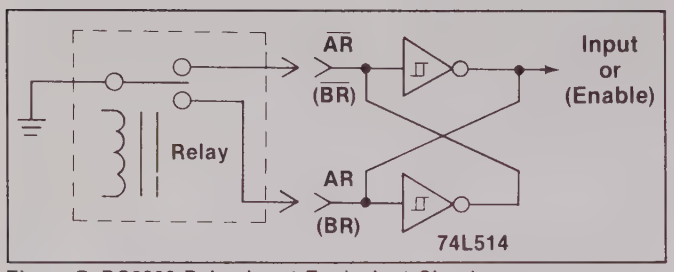

Figure 7. DC6300 Relay Input Equivalent Circuit.

OPTICALLY ISOLATED INPUT — DC6301

The DC6301 provides high voltage input isolation from externally generated common mode voltages. The Isolator LED leads are brought out directly to the user edge connector. User-supplied current limiting resistors may be installed at the signal source or on/between unused pins of the DC6301 user edge connector. Turning OFF the LED (Input A) increments the Counter. Turning ON the LED (Input B) changes the state of the Count Enable. Drive currents of 5 to 20mA may be used. The equivalent circuit is shown in Fig. 8.

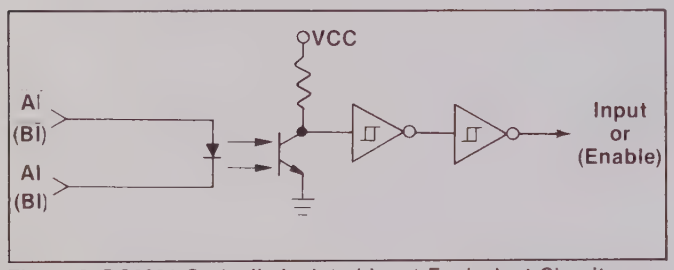

Figure 8. DC6301 Optically Isolated Input Equivalent Circuit.

ANALOG INPUTS — DC6302

This version of the DC63XX offers a high impedance input to a comparator with trigger voltage adjustment provided by a potentiometer, variable from +10V to −10V. The comparator is provided with 100mV of input hysteresis. The Counter advances on the positive transition of Input A. The Enable changes on the negative transition of B. The equivalent circuit is shown in Fig. 9.

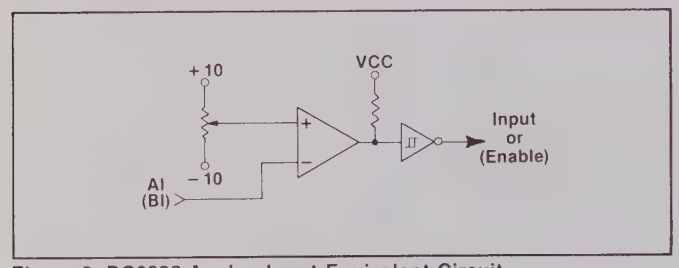

Figure 9. DC6302 Analog Input Equivalent Circuit.

EXPANDER CARD — DC6310

The maximum counting capacity for the basic CTC is 2^{16}-1 or 65,535. This capacity may be increased indefinitely by adding Counter Expander cards in cascade. Each additional Expander card adds another 16 bits to the Basic Counter for a capacity of 2^{32}-1, or over 4 billion for one additional Expander.

The Expander cards may be plugged into any slot in the ANDS5400 system. Each card must be connected to its adjacent cards by three wires on the user edge connector.

Fig. 10 shows connections for a typical expansion counting system of one basic and two Expander cards.

Expander cards may be preset to a certain count in the same manner as the basic CTC. Note that they must be addressed according to their card slot position in the ANDS5400. When presetting or reading data from a multicard Counter, Read operations should be made on the most significant word first and the least significant word (basic Counter card) last.

Expander cards have no time base, status register or interrupt capability. All Counters are reset simultaneously from the basic card Status Register or by reading the LSB Counter word.

If no Expander Card is used, Pins 7 and H must be jumpered together externally on the CTC User connector.

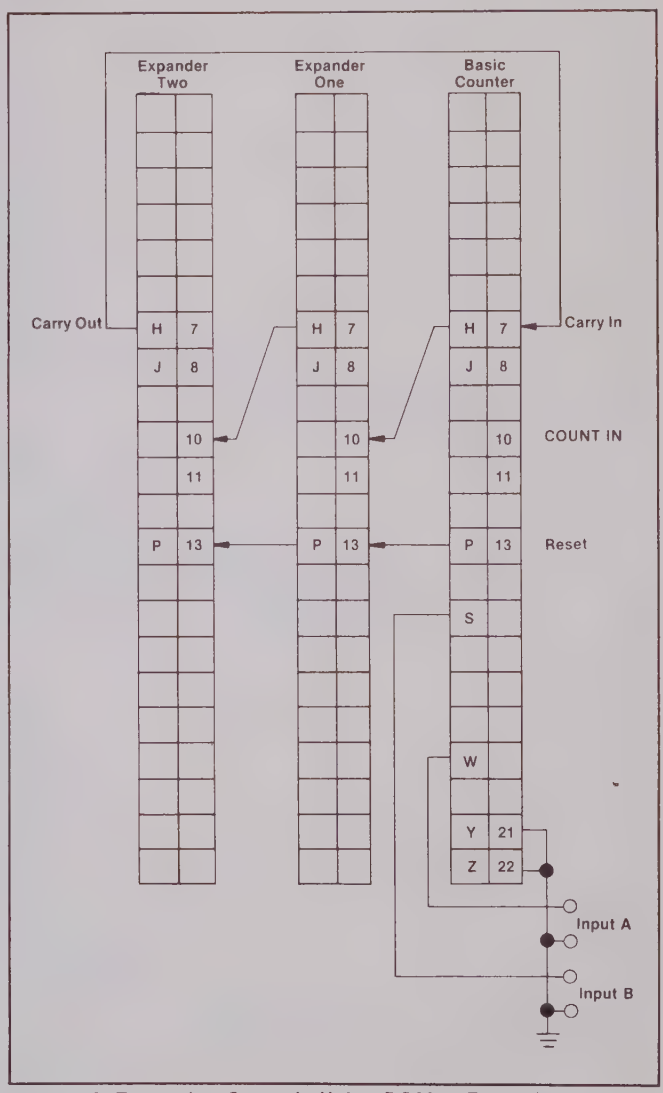

Figure 10. Expansion Cascade Using DC6310 Expander Cards.

TIME BASE — DC6320

The CTC card may be configured with time base only. As such, it has no counters, input conditioning, or interrupt logic. It does have a Status Register of one bit (D16), Write Only, for resetting the Time Base to zero (see status register description). Once initialized, f_{out} will be a constant frequency output (period) whose repetition rate is controlled by the clock rate (Internal or external) and programmed divisor. Frequency or period is measured from falling edge to falling edge. The Time Base and Mode Register may be read and loaded as in the basic CTC; however, the mode bits (D11 and D12) have no control function.

OPERATING MODES

D11 = MB
D12 = MA — Mode Select — See Table 4.

Frequency Count Input A, Internal Gate MB = 0, MA = 0

This Mode connects Input A to the Counter input and the Time Base output to the Counter Enable input. If the Time Base is programmed for a 1-second gate time, the number in the Counter at the end of that time will equal the frequency of A in Hz. If interrupts are enabled, an interrupt will be generated. The counter is advanced on the **positive edge** of the signal.

Count Preset A **MB = 0, MA = 1**

This Mode connects Input A to the Counter input, and the Counter Enable input to the Carry output. If a number is preset into the Counter, the CTC will count Input A until a carry occurs; then it will stop and, if interrupts are enabled, an interrupt will be generated. The complement of the desired number of counts must be preset into the Counter. The Counter is advanced on the **positive** edge of the signal.

Frequency Count A, External Gate **MB = 1, MA = 0**

This Mode is the same as Mode Zero except that the Counter Enable is connected to Input B instead of the Time Base. The Gate period will be between **negative transitions** of Input B. If interrupts are enabled, an interrupt will be generated at the end of the counting period.

Time B **MB = 1, MA = 1**

This Mode connects the Time Base to the Counter input, and Input B to Counter Enable. If the Time Base is programmed for 1kHz, the Counter output will equal the time between **negative transitions** of Input B in milliseconds. If interrupts are enabled, an interrupt will be generated at the end of the timing sequence.

MB	MA	Mode	Description
0	0	0	Count A Internal Gate
0	1	1	Count Preset A
1	0	2	Count A External Gate
1	1	3	Time B

Table 4. Mode Selection.

STATUS REGISTER

The 3-bit Status Register controls resetting of the CTC and indicates the state of the Done bit. The Done bit is tested to determine if operation is complete when the interrupt is disabled. The 3-bit word is shown in Fig. 4.

(D16) 1 = Reset. When set, this bit resets the Counter to zero, resets the Time Base f_{out} line to a high level, and initiates one counting sequence. The reset pulse is available as a 10μsec positive pulse at the user edge connector (see Fig. 11).

(D15) 1 = Enable. This bit enables the Auto Reset feature of the CTC. This feature automatically resets the Counter and starts a new measurement sequence whenever the contents of the Counter are read onto the ANDS5400 bus.

(D14) 1 = count in progress 0 = counting completed. This is a Read Only bit that indicates when the CTC has completed a count sequence.

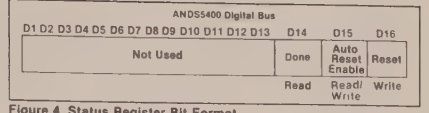

Figure 4. Status Register Bit Format.

INTERRUPT REGISTER

This 2-bit register is used for controlling CTC interrupts on the ANDS5400 bus. The register is detailed in Fig. 5.

(D16) Interrupt Enable — 1 = Enable. This bit controls interrupt generation on the CTC. When equal to zero, it prevents the card from asserting the request line and maintains the priority chain to lower priority cards. This bit is set to the zero state (disabled) during the system power up sequence.

(D15) Trigger Interrupt Request — 1 = Trigger. With D16 enabled, this bit generates an interrupt request from the card for testing purposes.

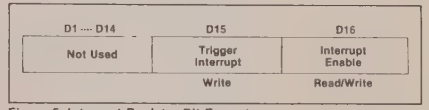

Figure 5. Interrupt Register Bit Format.

INPUT CONDITIONING

A wide variety of input conditioning permits the DC63XX to accept most types of input signals. Channels A and B may each have one of three types of signal conditioning. Input equivalent circuits are shown in the summaries below. Note that in all versions of this device, the Counter advances on the positive edge of the input and the Counter Enable changes state on the negative edge.

TTL DC6300

The DC6300 accepts TTL low power and low power Schottky inputs. Hysteresis is provided for greater noise immunity. Fig. 6 provides an input equivalent diagram for inputs AR and BR.

Should the user require terminated inputs, 50Ω for example, simply install 50Ω 10% carbon composition resistors (see Fig. 6) at R23 and R35 (near user edge connector pin 16).

Relay contacts may also be used to input the DC6300 for low speed counting applications. To implement the debounce circuitry, install jumpers E1 and E4 (near user edge connector pin 1). A Form C relay may then be used to input the DC6300, as shown in Fig. 7. Grounding $\overline{AR}$ or BR advances the Counter or changes the state of the Enable, respectively.

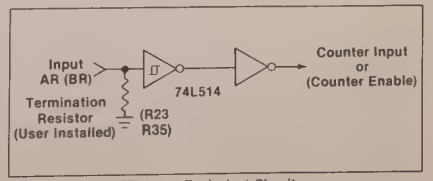

Figure 6. DC6300 TTL Input Equivalent Circuit.

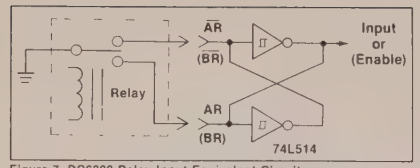

Figure 7. DC6300 Relay Input Equivalent Circuit.

OPTICALLY ISOLATED INPUT — DC6301

The DC6301 provides high voltage input isolation from externally generated common mode voltages. The Isolator LED leads are brought out directly to the user edge connector. User-supplied current limiting resistors may be installed at the signal source or on/between unused pins of the DC6301 user edge connector. Turning OFF the LED (Input A) increments the Counter. Turning ON the LED (Input B) changes the state of the Count Enable. Drive currents of 5 to 20mA may be used. The equivalent circuit is shown in Fig. 8.

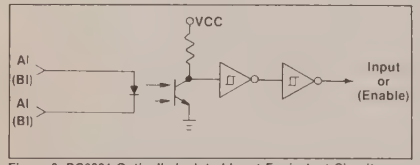

Figure 8. DC6301 Optically Isolated Input Equivalent Circuit.

ANALOG INPUTS — DC6302

This version of the DC63XX offers a high impedance input to a comparator with trigger voltage adjustment provided by a potentiometer, variable from +10V to −10V. The comparator is provided with 100mV of input hysteresis. The Counter advances on the positive transition of Input A. The Enable changes on the negative transition of B. The equivalent circuit is shown in Fig. 9.

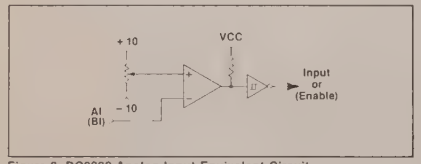

Figure 9. DC6302 Analog Input Equivalent Circuit.

EXPANDER CARD — DC6310

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Fig. 10 shows connections for a typical expansion counting system of one basic and two Expander cards.

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Expander cards have no time base, status register or interrupt capability. All Counters are reset simultaneously from the basic card Status Register or by reading the LSB Counter word.

If no Expander Card is used, Pins 7 and H must be jumpered together externally on the CTC User connector.

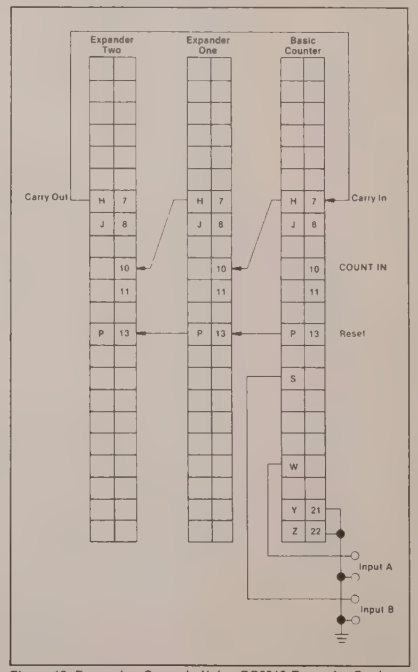

Figure 10. Expansion Cascade Using DC6310 Expander Cards.

TIME BASE — DC6320

The CTC card may be configured with time base only. As such, it has no counters, input conditioning, or interrupt logic. It does have a Status Register of one bit (D16), Write Only, for resetting the Time Base to zero (see status register description). Once initialized, f_{out} will be a constant frequency output (period) whose repetition rate is controlled by the clock rate (Internal or external) and programmed divisor. Frequency or period is measured from falling edge to falling edge. The Time Base and Mode Register may be read and loaded as in the basic CTC; however, the mode bits (D11 and D12) have no control function.

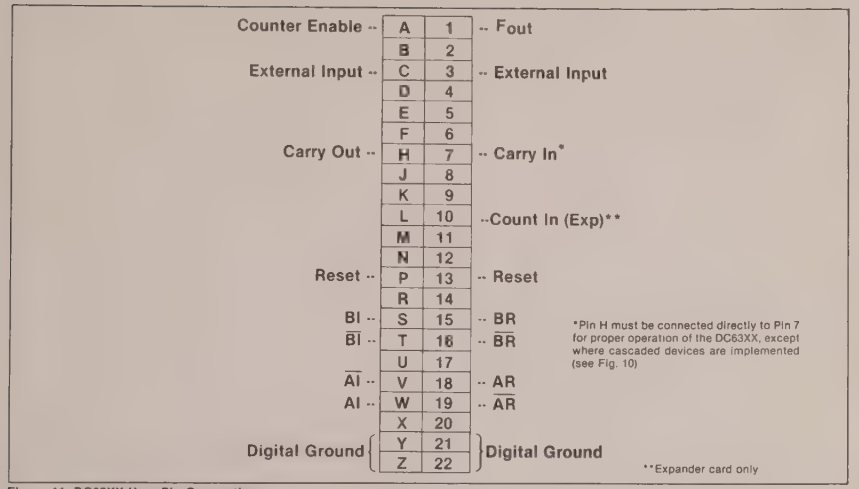

Figure 11. DC63XX User Pin Connections.

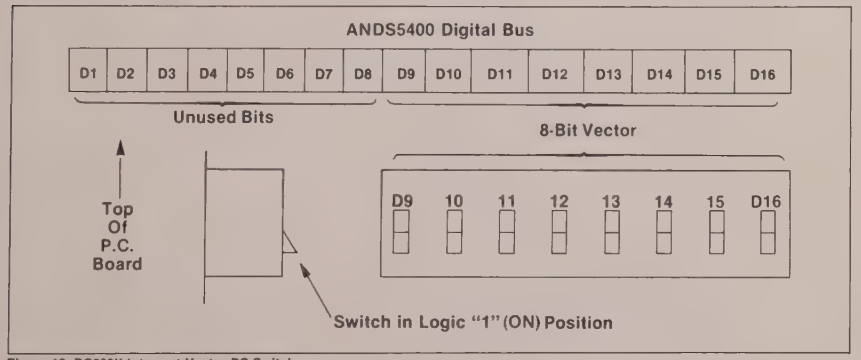
ANDS5400 Digital Bus
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16
Unused Bits
8-Bit Vector
Top Of P.C. Board
D9 10 11 12 13 14 15 D16
Switch in Logic "1" (ON) Position

Figure 12. DC630X Interrupt Vector PC Switch.

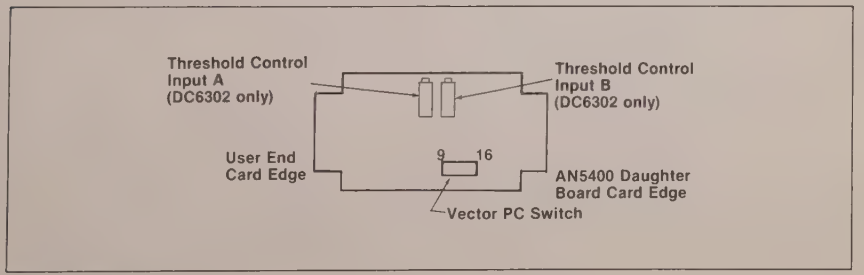

Figure 13. DC63XX PC Card Layout.

ORDERING GUIDE

Simply Specify For	Enter
TTL Input	DC6300
Optically Isolated Input Card	DC6301
Analog Input Card	DC6302
Expander Card	DC6310
Time Base Card	DC6320

ANALOGIC

ANALOGIC CORPORATION ■ Audubon Road ■ Wakefield, Massachusetts 01880
Tel. (617) 246-0300 ■ TWX (710) 348-0425 ■ Telex 94-9307
ANALOGIC INTERNATIONAL ■ Audubon Road ■ Wakefield, Massachusetts 01880
Tel. (617) 246-0300 ■ TWX (710) 348-0425 ■ Telex 94-9307
ANALOGIC AG ■ Kanalstrasse 15 ■ Postfach CH-8152 ■ Glattbrugg ■ Switzerland
Tel. (41) 1-810-0666 ■ Telex 845-59699
ANALOGIC LIMITED ■ 66 High Street ■ Weybridge, Surrey KT13 8BN ■ England
Tel. (44) 932-41251 ■ Telex 851-928030
ANALOGIC REGIONAL OFFICES ■
Cincinnati, Ohio (606) 371-0064 ■ San Jose, Calif. (408) 247-6401
Tustin, Calif. (714) 838-7243 ■ Garland, Texas (214) 681-0483
Houston, Texas (713) 777-6360

AVAILABLE FROM:

Bulletin No. 16-100154 REV. 0

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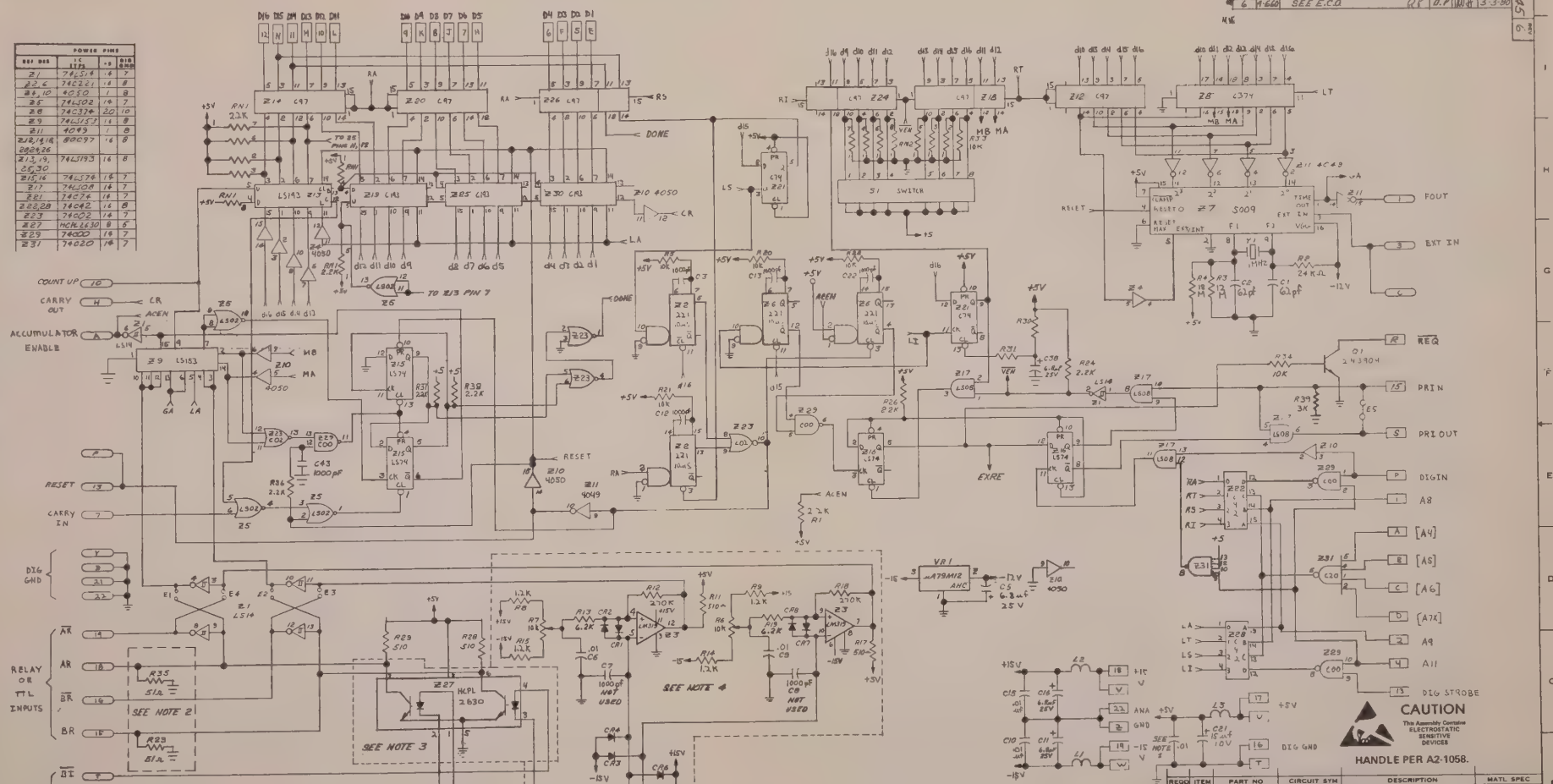
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPR	DATE
3	4634	SEE E.C.O.	[illegible]	D.P.	L.M.	2-8-77
3A	4803	SEE E.C.O.	R.T.	D.P.	L.M.	4-6-79
3B	4892	ENG. UPDATE	R.T.	D.P.	L.M.	8-28-79
4	4-5201					
5	4-569	SEE E.C.O.	R.T.	D.P.	L.M.	12-4-79
6	4-666	SEE E.C.O.	R.T.	D.P.	L.M.	3-3-80

POWER PINS			
REF DES	I.C. TYPE	+5	GND
Z1	74LS14	14	7
Z2,6	74C221	16	8
Z4, 10	4050	1	8
Z5	74LS02	14	7
Z8	74C374	20	10
Z9	74LS153	16	8
Z11	4049	1	8
Z12,14,18, 20,22,26	80C97	16	8
Z13,19, 25,30	74LS193	16	8
Z15,16	74LS74	14	7
Z17	74LS08	14	7
Z21	74C74	14	7
Z2228	74C42	16	8
Z23	74C02	14	7
Z27	MCNL6300	8	6
Z29	74C00	14	7
Z31	74C20	14	7



CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES

NOTES:
1. C4, C14, C17-C20, C23-C37, C39-C42 .01μF
2. PARTS FOR SO.1 INPUT.
3. PARTS FOR DC6301.
4. PARTS FOR DC6302.
5. 5400 BACKPLANE CONN.
USER CONN

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PL10-8645	DC63XX		
NEXT ASSY	USED ON		
APPLICATION			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± DECIMALS ± ANGLES ±

MATERIAL

FINISH

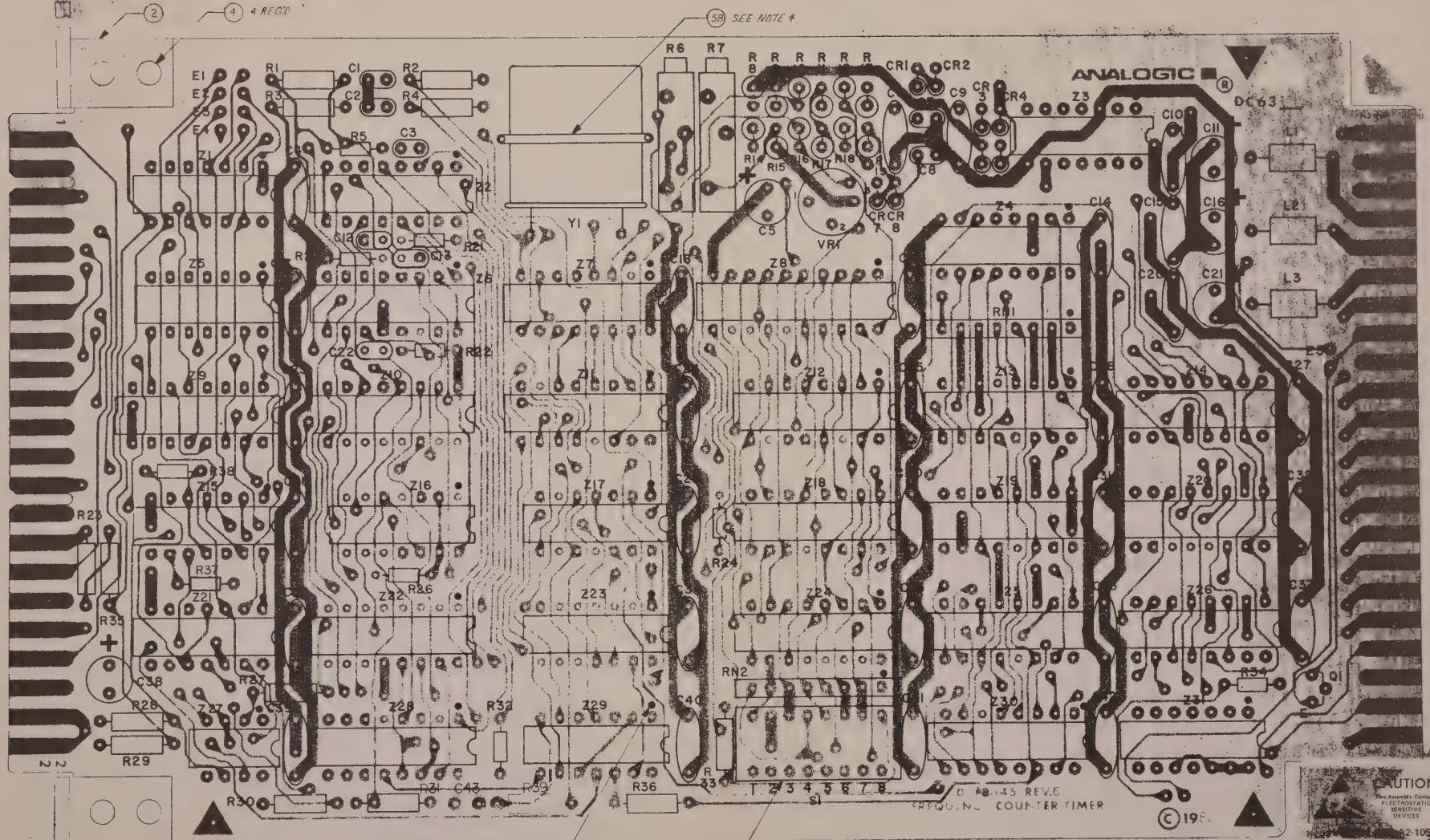
APPLICABLE SPECIFICATIONS

DRAWN	L. MULLER	DATE 4-1-78
CHECKED		
DESIGNED		10-24-78
ENGINEER		10-25-78
APPROVED		9-25-79
RELEASED		1/9/79
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

SCHEMATIC
FREQUENCY COUNTER TIMER
DC63XX

CODE IDENT NO	SIZE	5-8645	REV
31814	D		6
SCALE	ACCOUNT NO	SHEET 1 OF 4	



COMPONENT SIDE

NOTES:
1. FOR SCHEMATIC SEE DS-8645.
2. DOTS INDICATE PIN 1 OF I.C.'S & R.N.'S.
3. ASSEMBLE PER A2-1027.
4. INSTALL TEFLON SLEEVING AFTER WAVE SOLDING & CLEANING.

REVISIONS					
BY	ECO	DESCRIPTION	DWN	APPD	DATE
R.H.	8437	REV. 02	WA	WA	12-4-73
R.H.	8437	REV. 01	WA	WA	10-22-73

P: 10-8645	DC 63XX		
NEXT ASSY	USED ON		
APPLICATION			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON: DECIMALS .X ± .03, .XX ± .005, ANGLES ±
MATERIAL
FINISH

APPLICABLE SPECIFICATIONS

DRAWN	S.A. REPUCCI	DATE 10-9-73
ENGINEER	R. PERRY	10-23-73
ENGINEER	J. MULLER	10-24-73
ENGINEERING MGR	R. NANCE	10-25-73
QUALITY CONTROL	M. CARLINGHAM	10-26-73
PRODUCTION	E. KIMBALL	10-29-73
WEIGHT		

ANALOGIC

ASSEMBLY, FREQUENCY COUNTER TIMER DC 63XX

CODE IDENT NO 31814 SIZE D DWG NO 7-8645

SCALE 4/1

13
Digital Output

Card Number	Drawing Number	Title
DC6510	—	Digital Output Modules Data Sheet
DC6500/DC6510	C5-7445	DC6500/DC6510 32 Channel Digital Output Modules Schematic
DC6500/DC6510	D7-7445	DC6500/DC6510 32 Channel Digital Output Modules Assembly
DC66XX	—	DC66XX Digital Output Module Data Sheet
DC66XX	C5-7446	DC66XX Isolated Digital Output Module Schematic
DC66XX	D7-7446	DC66XX Isolated Digital Output Module Assembly
DC6700	—	DC6700 8 Channel Relay Card Data Sheet
DC6700	C5-8634	DC6700 8 Channel Relay Board Schematic
DC6700	D7-8634	DC6700 8 Channel Relay Board Assembly

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DC6510

DIGITAL OUTPUTS FOR ANDS5400

GENERAL

The Analogic DC6510 is a digital output card featuring two 16-bit parallel output ports. It provides fully compatible operation for use in Analogic's ANDS5400 Data Acquisition and Distribution System. As illustrated in Fig. 1, the DC6510 provides data buffers, two 16-bit latches and two tri-state buffers. The tri-state buffers provide the capability of reading back the data stored in the 16-bit latch of either channel.

The DC6510 outputs are designed to drive directly either TTL or CMOS-type devices, as indicated in Fig. 2. Specified dynamic performance may be checked by means of the test load circuit shown in Fig. 3. Table 1 shows pin assignments for the DC6510.

SPECIFICATIONS

Output Current
High (VOH = 3.4V): **1.5mA**
Low (VOL = 0.4V): **14mA (minimum)**

Output Voltage
High (IOH = 0): **5 volts**
Low (IOL = 14mA): **0.4 volts**

Propagation Delay
(CL = 15pF, RL = 400Ω): **130 nanoseconds**

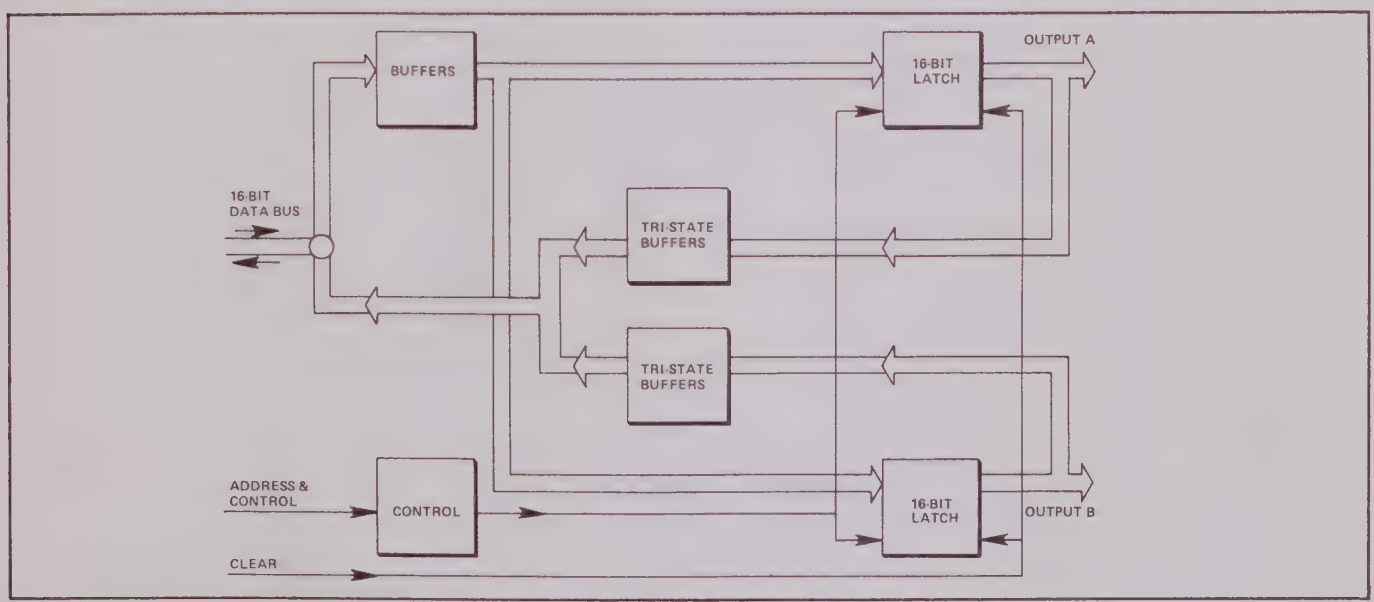

Fig. 1. DC6510 Digital Outputs Module Block Diagram.

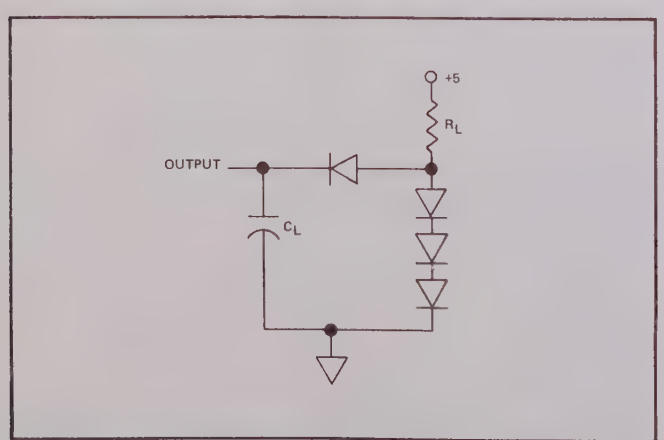

Fig. 2. DC6510 Equivalent Output Stage.

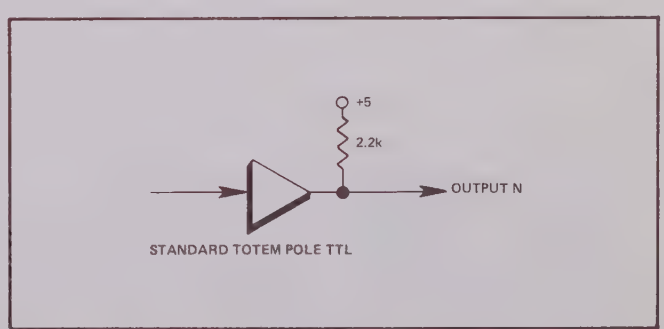

Fig. 3. DC6510 Output Test Load Circuit.

ANALOGIC®
...The Digitizers

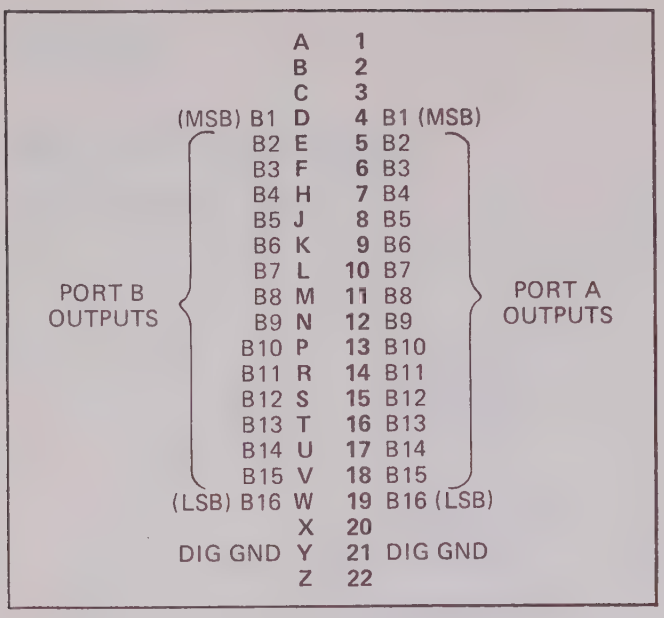

Table 1
User Pin Assignments (DC6510)

ADDRESSING

The address structure of the ANDS5400 provides complete flexibility of configuration and installation. Table 2 details the addresses of devices installed in a given enclosure. To determine the absolute address of this device, simply add the address indicated below to the enclosure address in the Digital Output Mode (See ANDS5400 Manual).

J1	0, 2	J9	40, 42
J2	4, 6	J10	44, 46
J3	10, 12	J11	50, 52
J4	14, 16	J12	54, 56
J5	20, 22	J13	60, 62
J6	24, 26	J14	64, 66
J7	30, 32	J15	70, 72
J8	34, 36	J16	74, 76

Table 2
Address Locations (Octal)

ANALOGIC®

ANALOGIC CORPORATION ■ Audubon Road ■ Wakefield, Massachusetts 01880
Tel. (617) 246-0300 ■ TWX (710) 348-0425 ■ Telex 94-9307
ANALOGIC INTERNATIONAL ■ Audubon Road ■ Wakefield, Massachusetts 01880
Tel. (617) 246-0300 ■ TWX (710) 348-0425 ■ Telex 94-9307
ANALOGIC AG ■ Kanalstrasse 15 ■ Postfach CH-8152 ■ Glattbrugg ■ Switzerland
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Bulletin No. 16-100131 REV 1

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CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES

HANDLE PER A2-1058

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPR'D	DATE
2	4-480	SEE E.C.O.	JJ	[illegible]	11-18-77
3	4-594	UPDATED REVISION	KW	DP	12-28-77

SIZE C | 5-7445 | REV 3

PORT A

PORT B

+5

R1 3K

Q1 3904

R2 2.2K

CLEAR

LOAD A

LOAD B

READ A

READ B

DIG. GND.

C7 15µ 10V

C1-C6 .01µf (X6)

TYPE	IC	+5	GND
74174	Z1,2,3,4,5,6	16	8
80C97	Z7,8,9,10,11,12	16	8
4050	Z13,14,15	1	8
74C20	Z16,18	14	7

TYPE	IC	+5	GND
7420	Z17	14	7
4049	Z19	1	8

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PL10-7445	DC65XX
NEXT ASSY	USED ON
APPLICATION	

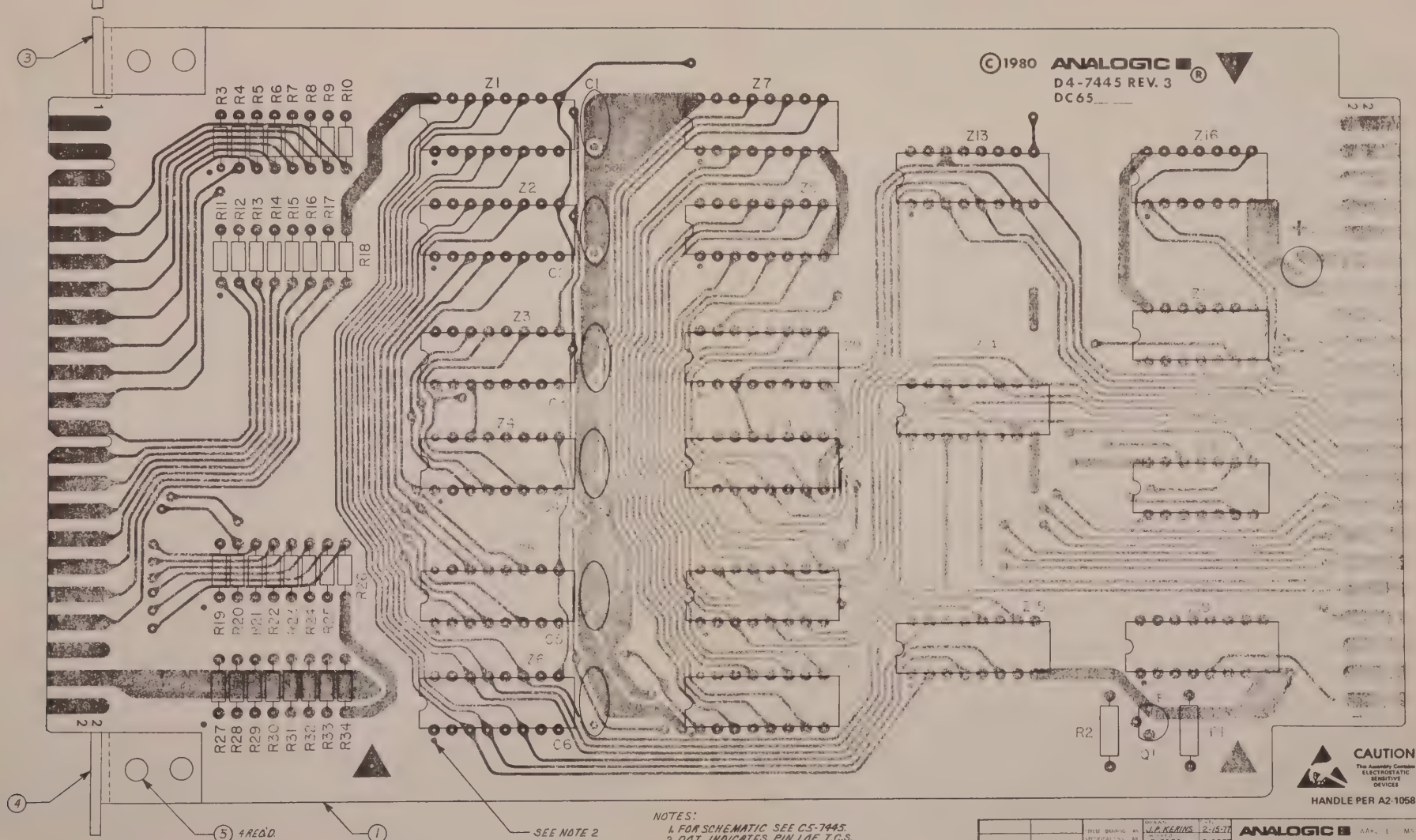
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

DRAWN	RWH	1-19-77
CHECKED	[illegible]	3-25-77
DESIGNER	[illegible]	3-25-77
ENGINEER	[illegible]	3-25-77
APPROVED	[illegible]	3/29/77
RELEASED	[illegible]	3/31/77
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

SCHEMATIC
DC6500, DC6510
32 CHANNEL DIGITAL OUTPUT

CODE IDENT NO	SIZE		REV
31814	C	5-7445	3
SCALE	ACCOUNT NO		SHEET 1 OF 1



NOTES:
1. FOR SCHEMATIC SEE CS-7445.
2. DOT INDICATES PIN 1 OF I.C.S.
3. ASSEMBLE PER A2-1027.
4. MAX. COMPONENT HEIGHT .500.

COMPONENT SIDE

REVISIONS				
REV	ECO	DESCRIPTION	DWN	APPL'S	DATE
3	4594	SEE E.C.O	PR. D.E.	SWB	2-11-80

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PL10-7445	DC65XX			
NEXT ASSY	USED ON			
APPLICATION				TOOL NO. 31814 SIZE D DWG NO. 7-7445 REV 3 SCALE 4:1 SHEET 1 OF 1

DC66XX
DIGITAL OUTPUT
FOR ANDS5400

GENERAL

The Analogic Model DC66XX is a 16-bit, optically isolated, parallel, digital data output card. The card is fully compatible with the ANDS5400 Data Acquisition System, and offers isolated digital control that can avoid troublesome ground loops, noise injection, and fault currents. A simplified block diagram of the DC66XX is shown in Fig. 1.

The card is available in two versions:

DC6620; with readback and on-board 2.2 k pullup
DC6630; with readback and open-collector output.

User pin connections are shown in Table 1. The output stage for a typical bit may be characterized as shown in Fig. 2.

The readback capability of the card allows software subroutines to check the actual state of the digital outputs readily without using memory storage or relying on previous data transfers.

SPECIFICATIONS

VCC (Supplied by user, measured with respect to output gnd.)	3-18 VDC
Leakage Current, Logic "1" (Bit Output = Vcc = 5.5V)	200μA. max.
Sinking Current, Logic "0" (Bit Output = 0.4V, Vcc = 4.5V)	20mA min.
Drive Capability (with Optional 2.2k, Vcc = 4.5V)	10TTL min.
Breakdown Voltage (From Output Gnd. to ANDS5400 Chassis Gnd.)	±500 VDC min.
Capacitive Coupling (From Output Gnd. to ANDS5400 Chassis Gnd.)	30pF max.
Propagation Delay (Thru Card, Worst Case, 1000pF Load)	50μs max.

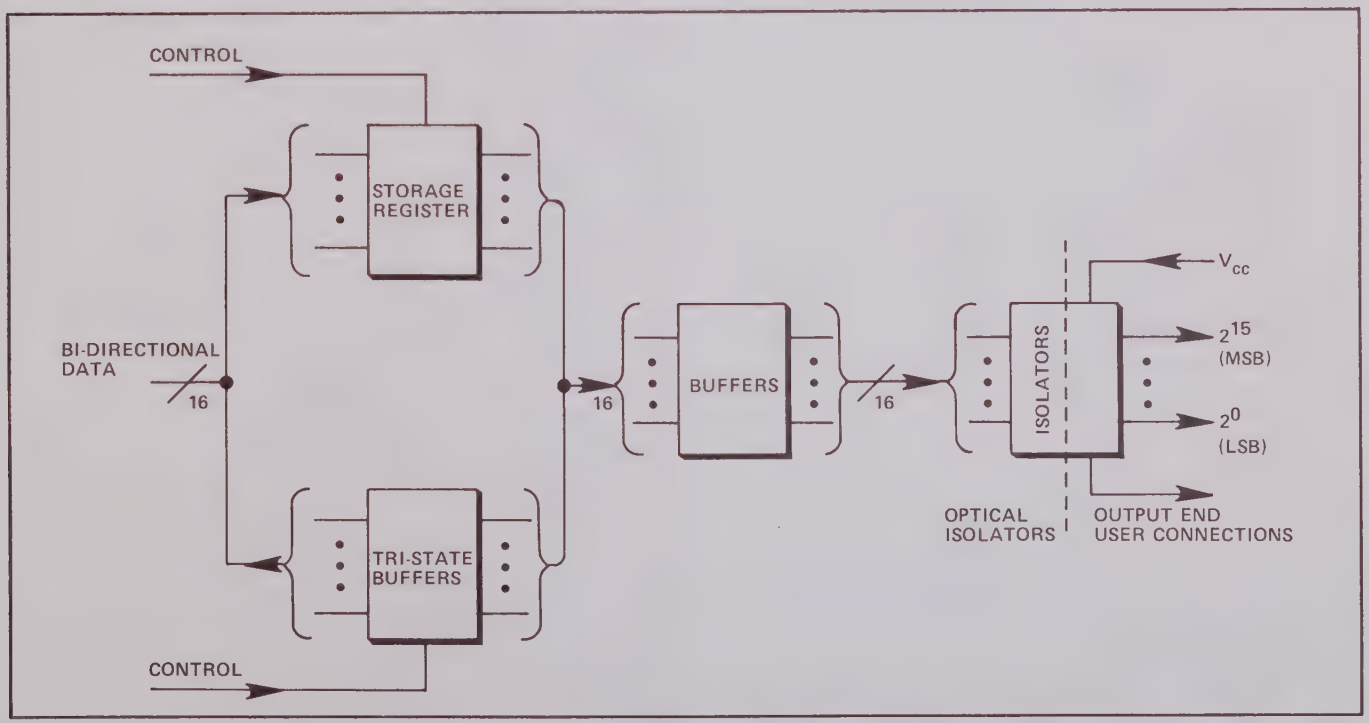

Fig. 1. DC66XX simplified block diagram.

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...The Digitizers

ADDRESSING

The address structure of the ANDS5400 provides complete flexibility of configuration and installation. Table 2 details the address of devices installed in a given enclosure. To determine the absolute address of this device, simply add the address indicated below to the enclosure address in the Digital Output Mode (See ANDS5400 Manual).

Table 1
DC66XX User Pin Connections

Output Gnd	A	1	Vcc
	B	2	
	C	3	
	D	4	2^0 Out (LSB)
	E	5	2^1
	F	6	2^2
	H	7	2^3
	J	8	2^4
	K	9	2^5
	L	10	2^6
	M	11	2^7
	N	12	2^8
	P	13	2^9
	R	14	2^{10}
	S	15	2^{11}
	T	16	2^{12}
	U	17	2^{13}
	V	18	2^{14}
	W	19	2^{15} Out (MSB)
	X	20	
	Y	21	
Vcc	Z	22	Output Gnd.

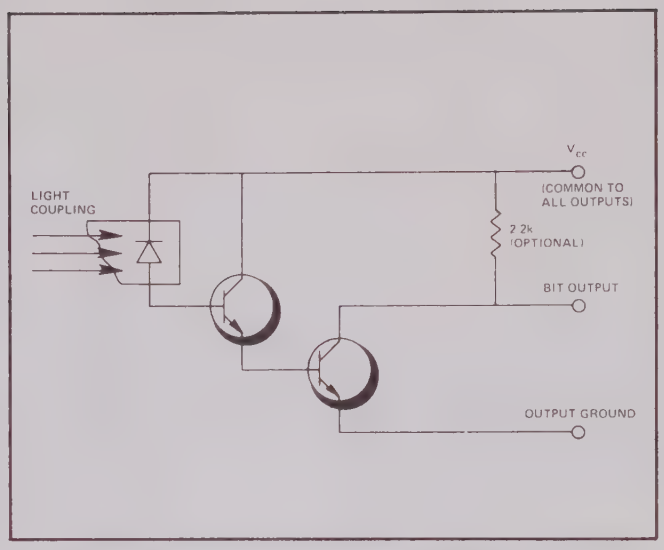

Fig. 2. DC66XX simplified schematic of optically isolated output stage.

Table 2
Address Locations

J1	0	J9	40
J2	4	J10	44
J3	10	J11	50
J4	14	J12	54
J5	20	J13	60
J6	24	J14	64
J7	30	J15	70
J8	34	J16	74

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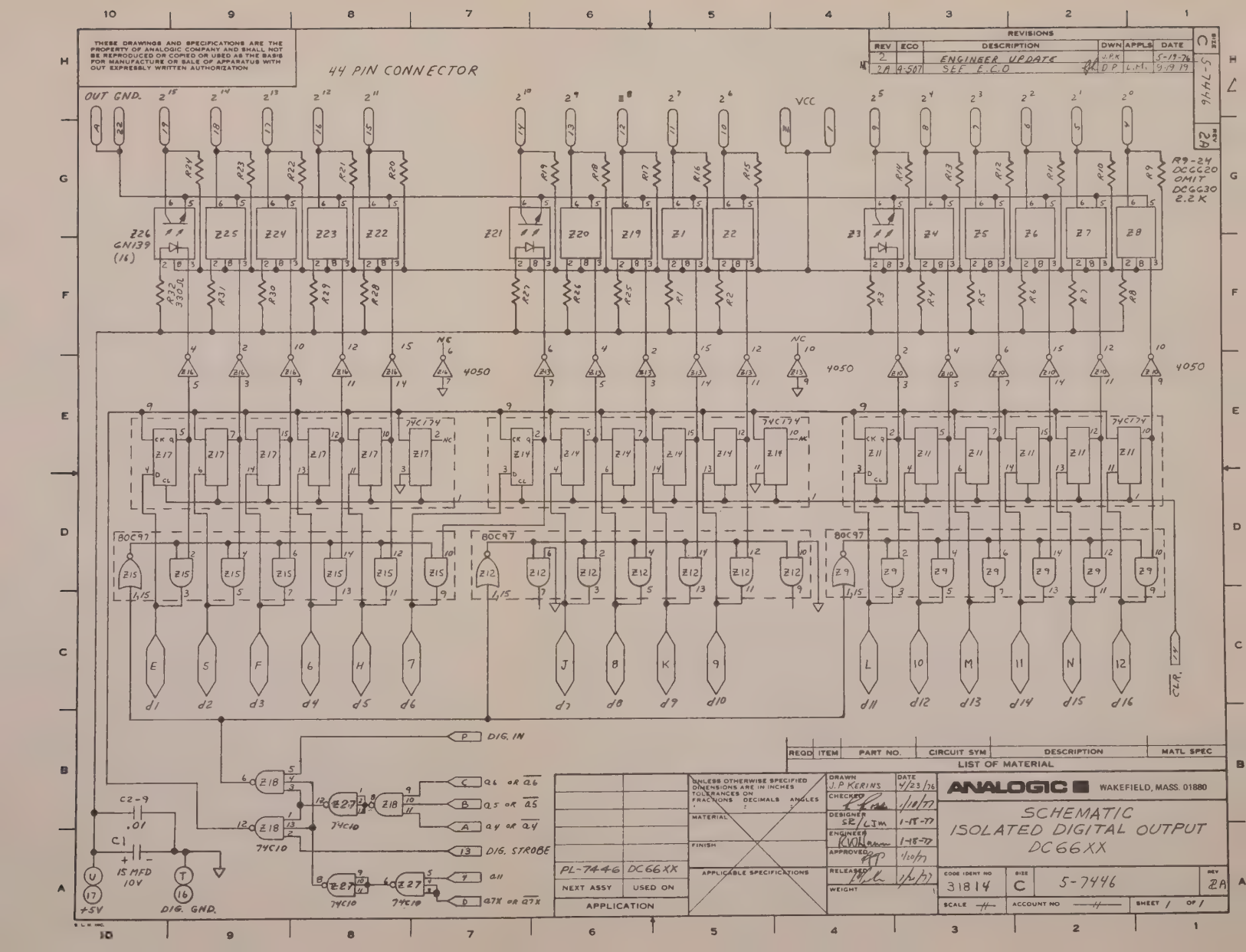
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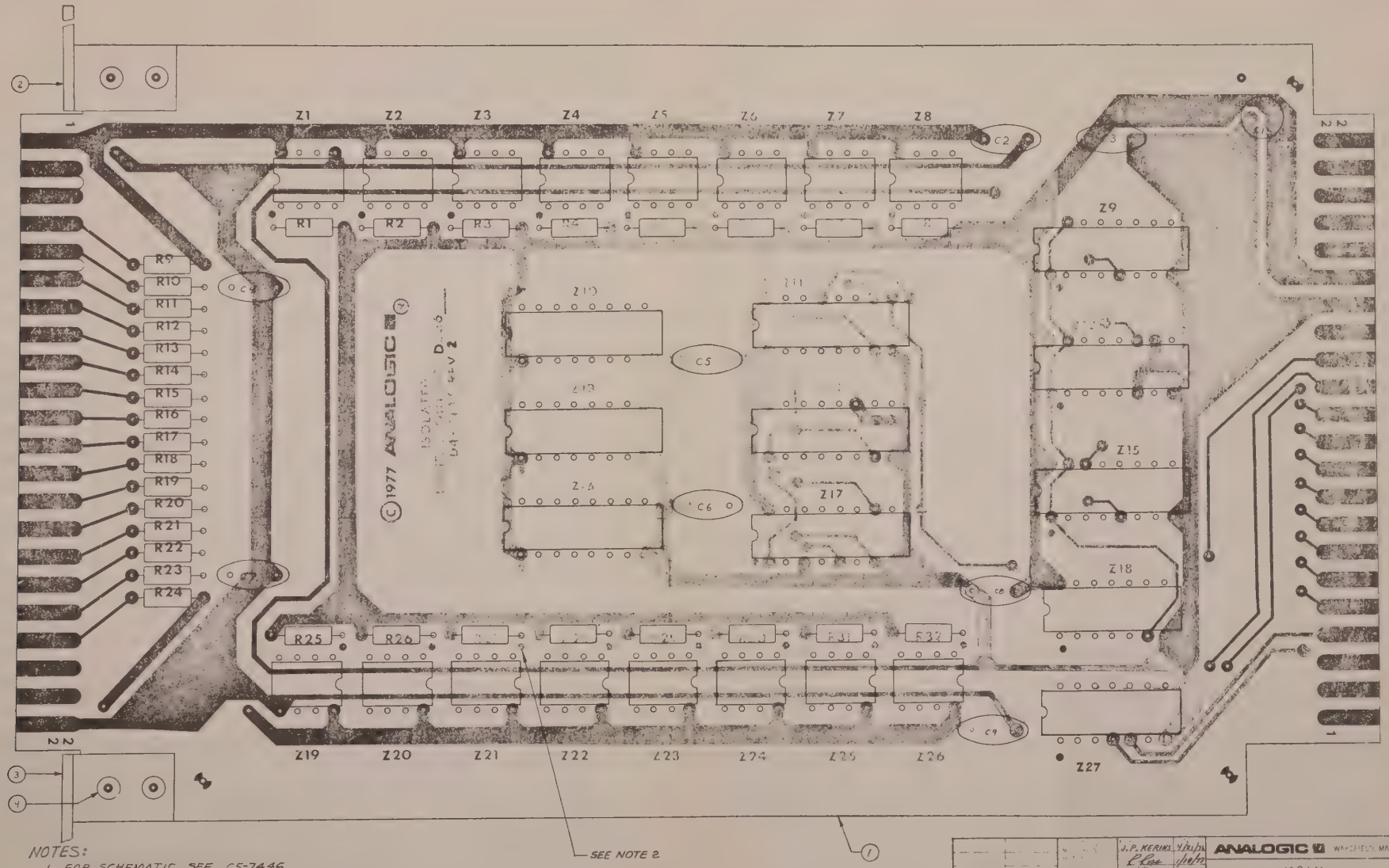
44 PIN CONNECTOR
REVISIONS
REV ECO DESCRIPTION DWN APPR'D DATE
2 ENGINEER UPDATE J.P.K. 5-19-76
2A 9-507 SEE E.C.O D.P. L.M. 9-19-79
SIZE C 5-7446 REV 2A
OUT GND.
VCC
Z26 GN139 (16)
4050
74C174
80C97
R32 330Ω
R9-24 DCGG20 OMIT DCGG30 2.2K
P DIG. IN
C2-9 .01
C1 15 MFD 10V
74C10
13 DIG. STROBE
11
7
DIG. GND.
+5V
LIST OF MATERIAL
REQD ITEM PART NO. CIRCUIT SYM DESCRIPTION MATL SPEC
ANALOGIC WAKEFIELD, MASS. 01880
SCHEMATIC
ISOLATED DIGITAL OUTPUT
DC66XX
PL-7446 DC66XX
NEXT ASSY USED ON
APPLICATION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN J.P KERINS 4/23/76
CHECKED 1/10/77
DESIGNER SR/LIM 1-18-77
ENGINEER KWH 1-18-77
APPROVED 1/20/77
RELEASED 1/24/77
WEIGHT
CODE IDENT NO 31814
SIZE C
5-7446
REV 2A
SCALE
ACCOUNT NO
SHEET 1 OF 1



NOTES:
1. FOR SCHEMATIC SEE CS-7446.
2. DOT INDICATES PIN 1 OF INTEGRATED CIRCUITS.
3. ASSEMBLE IN ACCORDANCE WITH A2-1027.

COMPONENT SIDE

		J.P. KERINS	4/21/77	ANALOGIC WAKEFIELD MASS 01880
		R Rose	1-18-77	ASSEMBLY ISOLATED DIGITAL OUTPUT DC66XX
		R.W.H.	1-18-77	
		R.W.H.	1-18-77	
		RAP	1/20/77	
PL10-7446 DC66XX		P.M. Rose	1/20/77	31814 D 7-7446 2
APPLICATION				SCALE 4:1 ACCOUNT NO. SHEET 1 OF 1

DC6700

8-CHANNEL RELAY CARD FOR AN5400

GENERAL DESCRIPTION

The Analogic model DC6700 is an 8-channel relay user card for the AN5400 Data Acquisition System. The card provides to the user 8 normally open relay contacts, which are high-voltage isolated and R.C.-protected against arcing. The user may supply coil power to the external relays, or make use of the internal +5 volt or +15 volt power supply. The card is offered in dry contact and Mercury wetted versions with coil voltage of 5, 12 or 24 volts.

Dry (Standard)	5 volt coil	DC6700
	12 volt coil	DC6701
	24 volt coil	DC6702
Mercury Wetted	5 volt coil	DC6710
	12 volt coil	DC6711
	24 volt coil	DC6712

OPERATION

The Analogic model DC6700 relay card is addressed in a manner identical to a single channel DAC card. The lower (LSB) 8 bits of data control the states of latches, which are buffered with high voltage, high current open collector drivers to the relay coils. Clamp diodes are used for transient protection on the coils.

The state of each relay may be read back into the AN5400 digital bus in a manner identical to that used for digital inputs. When power is applied to the card, all relays will be initially open. This reset condition lasts approximately 70ms, and thereafter the relays may be operated normally. For systems that are powered on automatically, the reset condition may be read back on bit D8 of the digital bus to indicate when the relays are ready to be operated. The relays may also be reset to the open condition by the system clear (CLR) signal. Figure 1 details the 16-bit data word controlling the relays.

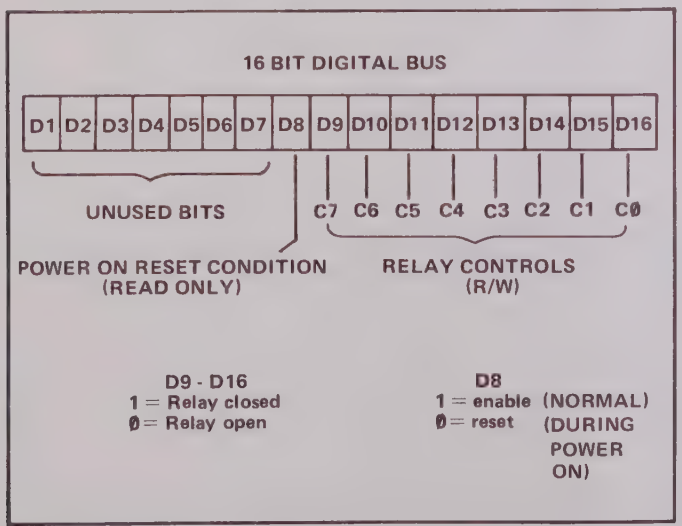

16 BIT DIGITAL BUS
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16
UNUSED BITS
C7 C6 C5 C4 C3 C2 C1 C0
POWER ON RESET CONDITION (READ ONLY)
RELAY CONTROLS (R/W)
D9 - D16
1 = Relay closed
0 = Relay open
D8
1 = enable (NORMAL)
0 = reset (DURING POWER ON)

Figure 1. Data Word.

DC6700 ELECTRICAL SPECIFICATIONS:

A. Standard Contact

TYPE	SPST N.O.
Rating	100VA (Res) 220 VAC, DC 2 Amps
Contact Resistance	50mΩ
Contact Bounce	<2ms
Expected Life	10^6 @ 1A 30 VDC
Breakdown Voltage	1,000 V RMS Contact to Coil 750 V RMS Contact to Contact
Maximum Operation Speed	50 cps.
Coil Voltages	5/12/24 VDC
Coil Resistance ($T_A = 25°C$)	90/500/2KΩ
Coil Power (Relays Closed)	2.5 w/card

NOTE: When the internal system +5 volt supply is used, the total number of relay cards per box must be less than 8. When the internal system +15 volt supply is used, the total number of relay cards must be less than 6.

Contact Protection - .01 uf in series with 47Ω.

A. Mercury Wetted

TYPE	SPST N.O.
Rating	25 VA (Res) 100 VDC 1 Amp (switch) 2 Amp (carry)
Contact Resistance	100 mΩ
Contact Bounce	NONE
Expected Life	40×10^6 1 Amp 25 VDC
Breakdown Voltage	1000 VDC Contact to Coil 1000 VDC Contact to Contact
Max. Operating Speed	100 Hz
Coil voltages	5/12/24 VDC
Coil Power (Relays Closed)	4 w/card

NOTE: When the internal +5 volt system supply is used, the total number of relay cards per box must be less than 5.

When the internal +15 volt system supply is used, the total number of relay cards per box must be less than 3.

Contact Protection - .01uf in series with 47Ω.

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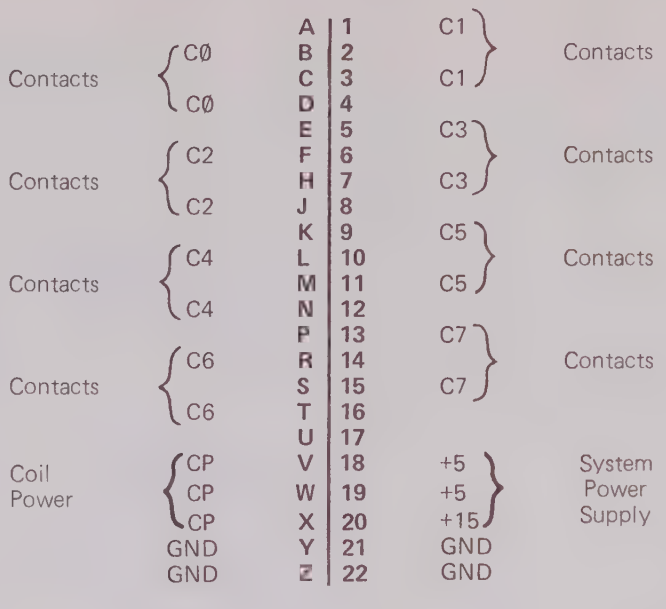

NOTE: For internal +15V operation, jumper X to 20.
For internal +5V operation, jumper V, W to 18, 19.

Figure 2. User Pinout.

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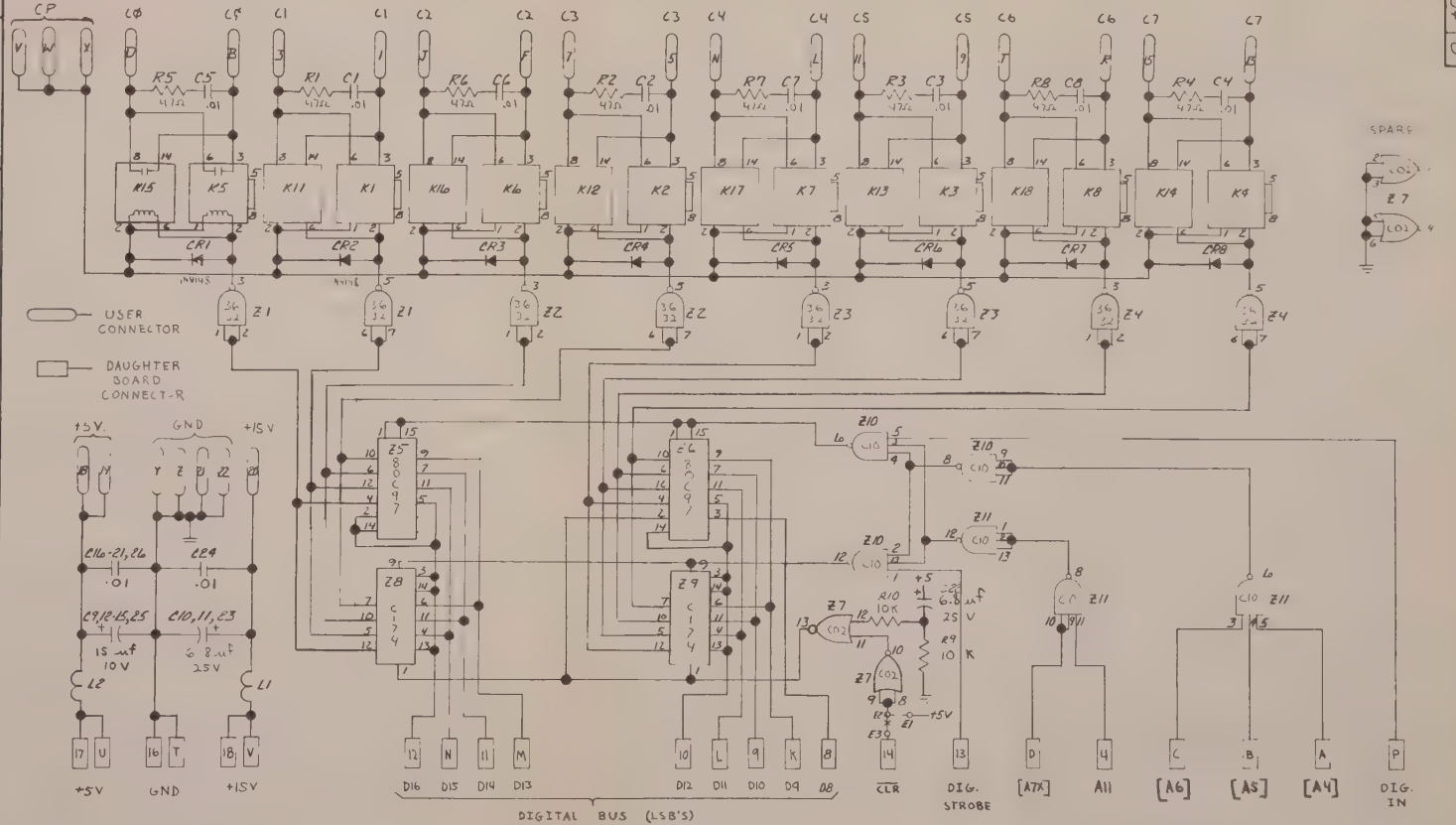
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

SIZE C 5-8634 REV 0



NOTE:
CUT ETCH E2-E3 AND JUMPER E1-E2 TO DISABLE CLEAR.

PL10-8634	DC67XX
NEXT ASSY	USED ON
APPLICATION	

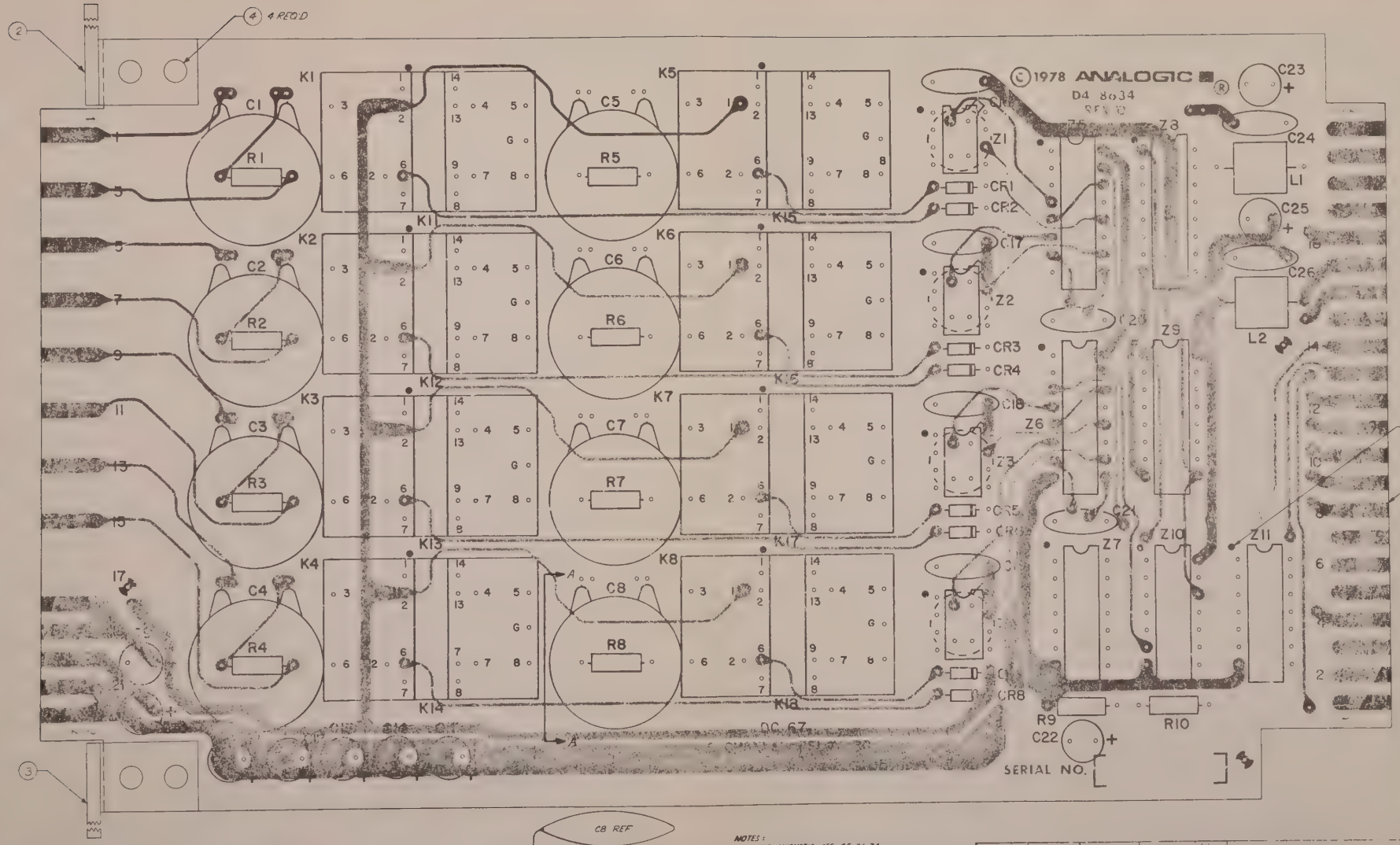
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .X± .XX± ANGLES .XX±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	L. J. MULLER	5-5-78
CHECKED		5-5-78
ENGINEER		5-5-78
ENGINEERING MGR		5-5-78
QUALITY CONTROL		6/18/78
PRODUCTION		7/3/78
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

AN 5400 DC 6700
8 CHANNEL RELAY BOARD

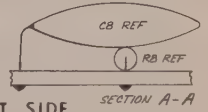
CODE IDENT NO	SIZE		REV
31814	C	5-8634	0
SCALE			SHEET 1 OF 1



REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPL'D	DATE
D					

7-8634

REV D



COMPONENT SIDE

NOTES:
1. FOR SCHEMATIC SEE CS-8634.
2. DOT INDICATES PIN OF I.C.'S AND RELAYS.
3. ASSEMBLE PER AE-1027.

J. LASPINA	3-14-78	
R. Ross	5-5-78	
L. Mullen	5-5-78	
W. Hamm	6-5-78	
EPS		

PL10-8634 DC 6700

NEW ASSY. USED ON

APPLICATION

ANALOGIC WAKEFIELD, MASS. 01880

ASSEMBLY
8 CHANNEL RELAY BOARD
DC 6700

31814	D	7-8634	10
SIZE	CODE IDENT NO.		SHEET 1 OF 1

14
Self-Test Card

Card Number	Drawing Number	Title
AC30X0	—	AC30X0 Self-Test Diagnostic Card Data Sheet
AC3000	—	Self-Test Program for AC3000 Card
AC30X0	D5-8617	AC30X0 Self-Test Card Schematic
AC30X0	D7-8617	AC30X0 Self-Test Card Assembly

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AC30X0 SELF-TEST DIAGNOSTIC CARD FOR AN5400

GENERAL DESCRIPTION

The Analogic Self-Test Card is a diagnostic tool for the AN5400 Data Acquisition System, for use under control of a computer test program. It provides the user with instant verification of system accuracy and functional operation in the field.

The Self-Test Card (STC) provides measurement of system power supplies, A/D converter accuracy and settling time. It provides 8 differential analog input channels for checking system D/A output cards. The unit also provides 8-bit input and output ports for digital testing. The analog inputs and digital inputs and outputs may also be used as normal data channels and can be controlled from the AN5400 front panel in the local mode.

The STC unit is a user-size PC card normally plugged into user slot J16 of the AN5400 master chassis. However, it is compatible with any user slot, and a system may be configured with more than one STC unit. Each STC unit may be custom-tailored for a particular A/D converter through the use of jumpers.

System tests that may be performed under software control are as follows:

Analog Tests

- Measurement of system power supplies +5V, +15V and −15V to 1% accuracy.
- Measurement of A/D and signal processor offset voltage.
- Measurement of A/D range accuracy with internal high stability reference voltage.
- Measurement of signal processor programmable gain accuracy with internal high stability reference voltage.
- Measurement of A/D linearity and center code voltages using internal system controlled integrator.
- Measurement of system slew rate and settling time for bipolar or unipolar A/D converters.

Digital Tests

- Complete verification of the system digital bus read/write operation.
- An internal function register provides readback of STC status and status of sample and hold cards if equipped.
- Test results are displayed (Pass or Fail) on two LED's visible from the rear of the chassis when the card is installed. Red is provided for "Fail" and green is provided for "Pass."

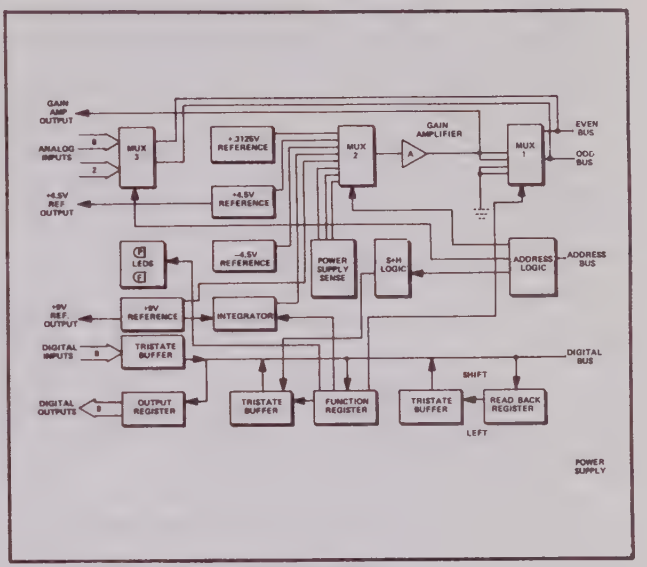

Fig. 1. Self-Test Card Block Diagram.

	Signal Return	A 1	Analog Ground	
	+9V Reference	B 2		
	AN0	C 3	AI0	
	AN4	D 4	AI4	
	AN10	E 5	AI10	
Analog Inputs	AN14	F 6	AI14	Analog Inputs
(High Side)	AN20	H 7	AI20	(Low Side)
	AN24	J 8	AI24	
	AN30	K 9	AI30	
	AN34	L 10	AI34	
	Gain Amp Output	M 11	Analog Ground	
	Analog Ground	N 12	High Reference Out +4.5V	
		P 13		
	DX0	R 14	DY0	
	DX1	S 15	DY1	
	DX2	T 16	DY2	
Digital Inputs	DX3	U 17	DY3	
	DX4	V 18	DY4	Digital Outputs
	DX5	W 19	DY5	
	DX6	X 20	DY6	
	DX7	Y 21	DY7	
	Digital Ground	Z 22	Digital Ground	

Fig. 2. User Pinout.

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CIRCUIT DESCRIPTION

The block diagram shown in Fig. 1, configures all major components of the Self-Test Card. Analog signals are routed using multiplexers 1 thru 3. Multiplexer 1 switches the even and odd bus lines separately to card ground or the gain amplifier. Multiplexer 2 selects one of three precise reference voltages, the integrator or one of three power supply derived voltages. Multiplexer 3 is an 8-channel differential multiplexer for external inputs.

The heart of the analog circuitry is a high precision, high stability, +4.5 volt reference. This reference, when measured through the system, will always read 90% of zero to full scale. The gain amplifier is jumpered to complement the range of the particular A/D converter. The 4.5 volt reference is also filtered and supplied to the user.

The low reference is a high stability source furnishing +0.3125 volts. When amplified by the gain amplifier, it will always read 1/16 full scale at the A/D converter. A High Stability +9V reference is also available to the user.

The minus reference is a stable −4.5 volts. The 5 volt power supply and +15 volt power supply are both attenuated to +4.5 volts for measurement. The −15 volts is attenuated to −4.5 volts.

The integrator is a highly linear 2 speed ramp generator that is computer controlled for automatic testing. The Gain Amp output is supplied to the user for measurement by a DVM when center code A/D tests are performed.

Potentiometers are provided for fine adjustment of amplifier gain and the +4.5-volt and +0.3125-volt references.

The system digital bus is tested by writing a 16-bit word into the Readback Register shown in Fig. 1. The register output is applied back to the bus, shifted one bit to the left through tristate buffers. Thus, the computer may compare the return data word against a shifted version of the transmitted data.

The Self-Test Card contains logic circuitry equivalent to that on a typical sample and hold card. The outputs of this logic are read back through the Function Register and indicate the sample and hold states of even and odd channels.

	(FUNCTION REGISTER F5 = 1)	ADDRESS BUS LSB'S					
		A8	A9	A10	A11	A12	Octal*
INTERNAL SOURCES	INTEGRATOR RAMP DOWN	0	0	0	0	N	0
	INTEGRATOR RAMP UP	0	0	0	1	N	2
	+5 SUPPLY SENSE	0	0	1	X	N	4
	+15 SUPPLY SENSE	0	1	0	X	N	10
	−15 SUPPLY SENSE	0	1	1	X	N	14
	HIGH REFERENCE OFFSET	1	0	0	0	N	20
	HIGH REFERENCE	1	0	0	1	N	22
	LOW REFERENCE OFFSET	1	0	1	0	N	24
	LOW REFERENCE	1	0	1	1	N	26
	MINUS REFERENCE OFFSET	1	1	0	0	N	30
	MINUS REFERENCE	1	1	0	1	N	32
	+9 VOLT REFERENCE	1	1	1	1	N	36
	(FUNCTION REGISTER F5 = Ø)	A8	A9	A10	A11	A12	Octal*
EXTERNAL ANALOG CHANNELS	CH. 0	0	0	0	X	N	0
	CH. 4	0	0	1	X	N	4
	CH. 10	0	1	0	X	N	10
	CH. 14	0	1	1	X	N	14
	CH. 20	1	0	0	X	N	20
	CH. 24	1	0	1	X	N	24
	CH. 30	1	1	0	X	N	30
	CH. 34	1	1	1	X	N	34

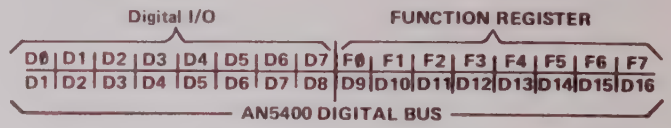
X = Don't Care, N = Don't Care for Differential. See AN5400 Manual.
*Relative to Card Slot Base Address.

(For 32/16 Patch Plugs)

Fig. 3a. A/D Addressing.

FUNCTION REGISTER

The Function Register is an 8-bit read/write register used to control and monitor the analog signal path, integrator speed, pass-fail LED's and the states of sample and holds in the system. When addressed, the Function Register appears as the low byte of a 16-bit word that includes the digital external I/O ports as the upper 8-bit byte. The structure of the 16-bit word is shown below:


Digital I/O
FUNCTION REGISTER
D0 D1 D2 D3 D4 D5 D6 D7
F0 F1 F2 F3 F4 F5 F6 F7
D1 D2 D3 D4 D5 D6 D7 D8
D9 D10 D11 D12 D13 D14 D15 D16
AN5400 DIGITAL BUS

FØ = (Read Only) Sample and hold odd, 1 = hold Ø = sample.
F1 = (Read Only) Sample and hold even, 1 = hold Ø = sample.
F2 = (R/W) Ramp speed, 1 = slow Ø = fast.
F3 = (R/W) PASS LED, 1 = on Ø = off GREEN.
F4 = (R/W) FAIL LED, 1 = on Ø = off RED.
F5 = (R/W) Internal/External A/D channels
1 = INTERNAL (MUX2).
Ø = EXTERNAL (MUX3).
F6 = (R/W) Even bus control (effective only when F5 = 1)
1 = bus to gain amp.
Ø = bus to card ground.
F7 = (R/W) Odd bus control (effective only when F5 = 1)
1 = bus to gain amp.
Ø = bus to card ground.
DØ = MSB of I/O port.
D7 = LSB of I/O port.

The Function Register enables programming the Self-Test Card for various tests without infringing on critical timing within a test. Note that when F5 = Ø the analog portion of the card becomes simply an 8-channel differential multiplexer addressed in the normal fashion. The 16-bit word formed by the Digital I/O and Function Register and the 16-bit word of the bus Readback Register are addressed exactly like a 2-channel DAC card. See Fig. 3.

When a CLEAR is issued to the system, the sample and hold circuits are reset to the sample state; the Function Register and the Digital Output Register are reset to zero.

The Readback Register cannot be cleared.

	ADDRESS BUS LSB'S					
	A8	A9	A10	A11	A12	Octal*
DIGITAL I/O AND FUNCTION REGISTER READBACK REGISTER	0	X	X	X	X	X	0
	1	X	X	X	X	X	2

X = Don't Care
*Relative to Card Slot Base Address.

(For D/A of 4 Patch Plugs)

Fig. 3b. D/A Addressing.

SELF-TEST CARD MEASUREMENT TECHNIQUES

In all measurements of gain, the AN5400 system must be programmed for differential gains on the Signal Processor.

Prior to any series of analog measurements, Multiplexer 1 must be programmed on the Self-Test Card to apply signal to the desired analog bus. This is done by digitally addressing the Function Register prior to loading, with the data needed to set the buses to the desired signals (see Function Register Section on page 2).

MEASUREMENT OF OFFSET IN A/D AND SIGNAL PROCESSOR

Program the Function Register to internal inputs (F5 = 1), by setting the even bus and the odd bus to card ground (F6 = F7 = Ø). Set up a differential gain of 1 on the Signal Processor. Make a conversion on any channel on the Self-Test Card. The result will be the combined offsets of the Signal Processor and the A/D converter.

If an AC260 Signal Processor is used, verify autozero operation by increasing gain to 8, differential. There should be no change in the measured offset.

MEASUREMENT OF A/D CONVERTER RANGE ACCURACY

Program the Function Register F5 = F6 = 1, F7 = Ø. For maximum accuracy, the offsets of two amplifiers on the Self-Test Card must be measured immediately prior to measurement of reference voltages so that they may be later subtracted.

This is done simply by addressing "High Reference Offset" channel, as shown in Fig. 3, waiting at least 1 msec. and making a conversion. Address "High Reference" channel, wait another 1 msec. and convert again. Subtract the first conversion from the second and the result will be 90% of zero to plus full scale.

MEASUREMENT OF PROGRAMMABLE GAIN ACCURACY ON AC260-EQUIPPED SYSTEMS

The same offset canceling procedure must be used as in the previous test. Address the "Low Reference Offset" channel, wait 1 msec. and convert. Address the "Low Reference" channel, wait 1 msec. and convert. Subtract the offset and the resulting data will be 1/16 of zero-to-full scale. Repeat this procedure with differential gains of 2, 4 and 8 on the AC260. Observe results of 1/8, 1/4 and 1/2 of zero to full scale, respectively.

MEASUREMENT OF SYSTEM SETTLING TIME

Since absolute accuracy is not normally important for this test, it is not necessary to subtract amplifier offsets. On bipolar converters, measure alternately between "High Reference" and "Negative Reference." To measure positive settling time, address the "High Reference", waiting at least 50 μsec. and convert. Address the "Negative Reference" momentarily and re-address the "High Reference." Wait 6 μsec. and convert. The resulting data should differ from the steady state reading by no more than .02% of FSR. Negative settling time may be measured in a similar manner. Systems with unipolar converters may be slewed between the "High Reference" and the "Low Reference." Settling should be within .02% of FSR in 6 msec. Settling time should be measured differentially first with the odd bus to ground and the even bus to the gain amp., and then with the buses reversed.

INTEGRATOR OPERATION

The integrator is an extremely useful device for checking the system A/D converter. For most tests, the Function Register should be set for the low integration speed (F2 = 1). The integrator direction is controlled by the A11 bit of the address bus. When the STC is unaddressed, the integrator ramps down to minus full scale and remains there.

CENTER CODE TEST

The analog voltage, represented by any particular code, may be measured by connecting a high impedance (>100 MΩ) DVM to the Gain Amp output and programming the following test.

Address "Integrator Ramp Up" and make continuous conversions until the A/D data is greater than the desired code. Immediately address "Integrator Ramp Down" and keep converting until data is less than the desired code. At this point, the ramp is reversed and the cycle is repeated. The output to the DVM is an averaged version of this sawtooth and represents the code center voltage, that is, the average of the voltages represented by the edge of the desired code and the edge of the code above. See Fig. 4.

In automatic testing of several code centers widely spaced, it is useful to use the high integrator speed to save time in positioning the integrator.

LOCAL LINEARITY TEST

Linearity about any particular code of interest may be observed by ramping the integrator 8 codes above and below the selected point and computing the number of conversions per code. Any inequalities indicate nonlinearities in the A/D converter.

HISTOGRAMS

A novel method of observing linearity over the entire range of the A/D converter is the histogram. The integrator is started below minus full scale and ramped to over plus full scale. Conversions are made continuously over the range. The data generated is examined to determine the number of times each code occurred. A table may be made to show the number of conversions on a particular code against the number of codes that appeared that many times. A typical histogram is shown in Fig. 5.

For a 12-bit converter, perfect linearity would be indicated by 4094 codes occurring the same number of times. Note that the end points of the range may not be considered, since they have no outer code edges. Missing codes are indicated by tallies in the zero column.

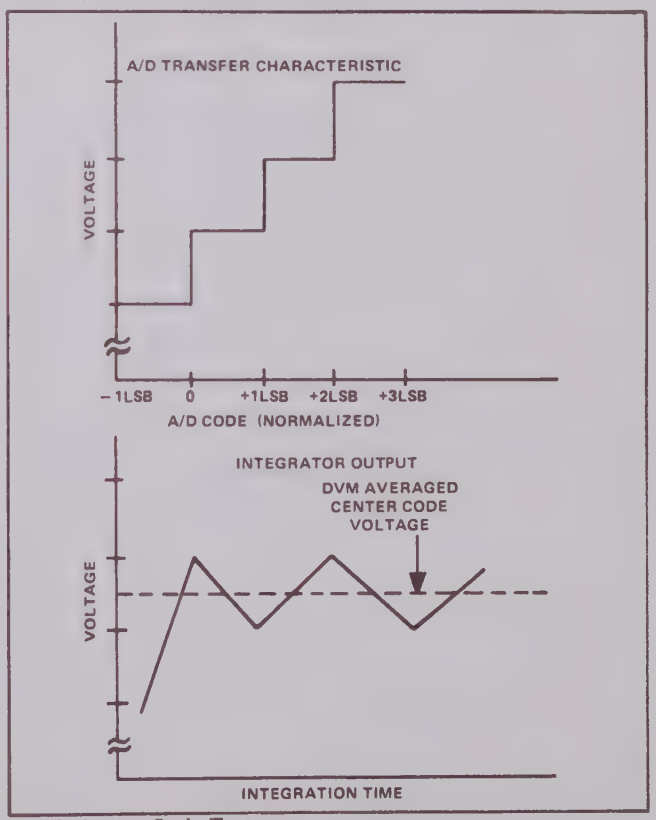


Fig. 4. Center Code Test.

+4.5-VOLT REFERENCE	
Accuracy*	±.001%
Temperature Coefficient*	±10 ppm/°C
Warm-Up Time	20 sec.
Stability Over 1000 Hours*	20 ppm
Noise Voltage ($10<f_o<10$ kHz)	<50 μV RMS
Output Impedance (User End)	100 Ω with .018 μF shunt
–4.5-VOLT REFERENCE	
Accuracy	±1%
Temperature Coefficient*	±50 ppm/°C
Warm-Up Time	20 sec.
Stability Over 1000 Hours*	20 ppm
Noise Voltage ($10<f_o<10$ kHz)	<50 μV RMS
+0.3125-VOLT REFERENCE	
Accuracy*	±.001%
Temperature Coefficient*	±10 ppm/°C
Warm-Up Time	20 sec.
Stability Over 1000 Hours*	20 ppm
Noise Voltage ($10<f_o<10$ kHz)	50 μV RMS
INTEGRATOR	
Speed	(2 speed) fast: ±17 V/sec. slow: ±.14 V/sec.
Linearity	±.001%
Gain Amp. Output Impedance (User End)	100 Ω
+9 V REFERENCE	
Accuracy	±5%
Temperature Coefficient	±10 ppm/°C
Output Impedance (User End)	100 Ω
EXTERNAL DIFFERENTIAL INPUTS	
Input Impedance	>100 M ohms
On Channel Leakage Current	<100 nA
Offset Voltage	<0.25 mV
Transfer Accuracy	0.01%
Settling Time to .02% FSR	8 μs (with 470 pF bus load capacitance)
Input Signal Range (Signal Plus Common Mode)	±11 volts
Overvoltage Ability	±25 volts, all inputs continuous. Power OFF or ON.

POWER SUPPLY SENSE

+5 volts attenuated to +4.5 volts ±1%
+15 volts attenuated to +4.5 volts ±1%
–15 volts attenuated to –4.5 volts ±1%
Noise voltage at any sense output <100 μV RMS at 120 Hz

*These parameters apply when card is measured with amplifier offset and drifts removed by software procedure.

DIGITAL OUTPUTS	
Fanout	2 TTL Loads
Output Low Current (Vol = .4 V)	3.6 mA
Rise Time	120 ns
Output High Voltage	5 volts
DIGITAL INPUTS	
Input Equivalent Circuit	CMOS input with 2.4 kΩ pull-up to V_{cc}.

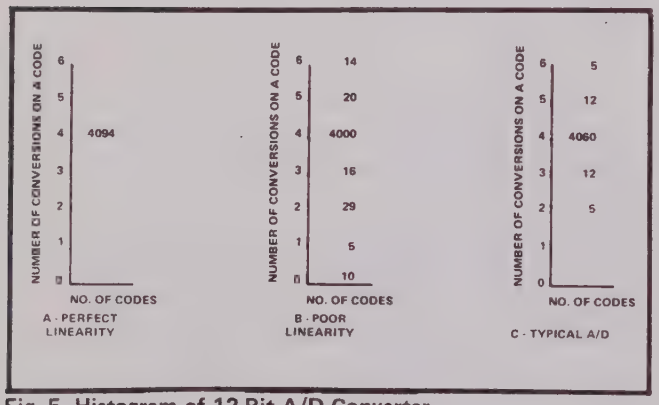


Fig. 5. Histogram of 12-Bit A/D Converter.

ORDERING CODE

The Self Test Card must be factory configured for the particular A/D converter used in the system. Order according to the table below:

STC	A/D Range	Card Gain
AC3000	0–10 V, ±10 V	2
AC3010	0–5 V, ±5 V	1
AC3020	0–10.24, ±10.24 V	2.048
AC3030	0–5.12, ±5.12 V	1.024

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SELF-TEST PROGRAM FOR AC3000 CARD

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GENERAL DESCRIPTION

The Analogic Self-Test Program for the AC3000 Card is a stand-alone program, furnished in two versions, and is compatible with either the DEC* PDP-11* or the LSI-11.* The prerequisites for operation are:

- A working PDP-11 or LSI-11 system, or Analogic ANDS 7000 system with at least 10 K of core or RAM.
- Console I/O device at address 177560 (CRT, Teletype, etc.)
- Loading device and loading program:
  1. Absolute loader & paper tape reader.
  2. RT-11 & mass storage device.
  3. RSX-11 & mass storage device.
- Analogic PDP-11/AN5400 Interface or LSI-11/AN5400 Interface or ANDS 7000/AN5400 system.
- Installed and functional AN5400 system with standard patch panels.
- A compatible version of the AC3000 Self-Test Card, installed in any user slot of the AN5400 system.

The Self-Test Program provides a complete and thorough check of the bus structure and A/D converter in the AN5400 system. The card simulates the three types of user cards available for the System: analog input, digital input and digital output. This software is not intended to test the Interface between the computer and the AN5400. It is suggested that the Analogic Diagnostic and Exerciser/Driver be operated with the system to verify proper Interface operation.

When started, the program prints: AN5400 SELF-TEST PROGRAM

Then: ENTER AN5400 BOX NUMBER (Ø-7) Ø

The user responds with the number of the chassis that contains the AC3000 card. Box Ø is the master chassis, and Box 1 is the first slave chassis.

ENTER SLOT NUMBER (1-16) 1

The user responds with the slot number within the selected chassis that contains the AC3000 card.

1 through 16 correspond to the printed slot numbers at the rear of the chassis.

ENTER A/D TYPE (A-J) I

The user response to A/D type is a single letter chosen from the following, to represent the voltage range of the A/D installed in the system:

A→	0–1
B	0–5
C	0–5.12
D	0–10
E	0–10.24
F	±1
G	±5
H	±5.12
I	±10
J→	±10.24

PROGRAMMABLE GAIN? Y

The user responds Y or N, depending upon whether or not the system contains a signal processor that has programmable gain. (Example: AC260 has programmable gain; AC262 does not.)

During the next interval, the software determines the number of bits available in the A/D converter (8, 10, 12, 13, 14, 15 or 16) and the type of coding (binary, offset binary or two's complement).

The program then prints NEXT > and awaits user entry of a test number according to the following table:

1. Digital Bus
2. Sample and Hold
3. A/D Offset
4. A/D Range
5. Read Power Supplies
6. Peak-to-Peak Noise
7. Slew Error
8. Common Mode Rejection Ratio
9. Signal Processor Gains
10. Missing Codes
11. A/D Linearity
12. Code Centers
13. Pass/Fail Lights
14. External Digital Output
15. External Digital Input
16. External Analog Inputs

These tests may be run in any order, but the numerical sequence represents a logical testing order for the system.

MEMORY REQUIREMENT: 10 K RAM minimum (does not include operating system). Uses 00000 - 45000.

LOADING PROCEDURE: Paper tape: Use standard procedure for absolute binary formatted tapes.

Floppy Disc: Discs are supplied with two object modules.

For LSI-11: STCPL. OBJ & COMPUT. OBJ.

For PDP-11: STCPP. OBJ & COMPUT. OBJ.

These two object modules are linked together by the user to create a load module. Starting address = 1000 for all versions of the program.

The program does not require any operating system, once initiated. The user cannot return control to an operating system once the program is entered.

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TEST NO. 1: DIGITAL BUS READ/WRITE TEST

During this test the Self-Test Card (STC) is written to as a digital output card and then read back as a digital input card. To prevent a successful test on a missing card due to capacitive storage of the data on the data bus, the STC performs a rotation on the data it receives. Thus, the data read back from the STC is the same as the data written to the card, rotated one bit to the left. During this test, all 65,536 bit combinations are checked and all errors are accumulated and listed. The normal operating time for this test is about one minute.

TEST NO. 2: SAMPLE AND HOLD TEST

During this test, the digital output addresses 4000, 4001, 4002 and 4003 are sent to the system. These commands should create defined responses in simultaneous sample and hold cards. To check this, the STC contains the same logic circuitry that is on a sample and hold card. After each command is issued, the STC circuitry is interrogated and checked. For each of the four commands, the form of the printout is as follows:

PART 1: ODD-SAMPLE, EVEN-SAMPLE
PASS

The printout indicated that, after the 4000 command, both the odd and even simultaneous sample and hold channels should be in the sample state, and the interrogation of the STC indicated that they were in the correct state. If an error had occurred in the odd channel logic, the printout would have been:

PART 1: ODD-SAMPLE, EVEN- SAMPLE
ODD-HOLD

The test continues in a similar fashion for the remainder of the four commands:

PART 2: ODD-HOLD, EVEN-SAMPLE
PASS
PART 3: ODD-SAMPLE, EVEN-HOLD
PASS
PART 4: ODD-HOLD, EVEN-HOLD
PASS

TEST NO. 3: MEASUREMENT OF OFFSET IN A/D CONVERTER

During this test, the STC is programmed to short the even and odd analog buses together with FET switches; a differential measurement is then made using the signal processor and A/D converter. The resulting data is converted into an equivalent voltage, based on the type of converter being used, and is printed. A typical printout would be as follows:

MEASUREMENT OF OFFSET IN A/D
SYSTEM WITH SHORTED INPUTS - 0.0048828 VOLTS

Several interesting points are noted with regard to this test:

1. Measurements made in this test and in all other tests are performed differentially, since grounding of the signal return line in the system is performed by the user and cannot be relied upon as an accurate reference for measurements on the STC.
2. This test may be performed repetitively, to adjust the signal processor or A/D converter offsets.
3. It should be kept in mind that the offset voltages measured in this test, are quantized by the A/D converter and all readings will be integer multiples of the LSB value. Thus in a good 12-bit ±10 volt system, a 2.4-millivolt offset will be read as either 0 volts or 4.88 millivolts.
4. Systems with unipolar converters may have special problems in this and other analog tests. If a reading from any A/D converter results in the lowest possible code from the converter, the message:

   OFF SCALE LOW

will be printed. In unipolar converter, the lowest code normally represents zero volts, but negative voltages will also result in the lowest code. In this test with a unipolar converter, only positive voltages will result in a voltage printout, while zero or negative voltages will result in the "Off-Scale Low" message. Alternatively, the Code Center Test, described under Test No. 12, can be used as a simple means of system calibration.

TEST NO. 4: A/D CONVERTER RANGE

During this test, a precision, stable voltage reference on the STC is measured by the A/D converter, and the result is printed. For a ±10 volt 12-bit converter, a typical printout would look as follows:

MEASUREMENT OF A/D CONVERTER RANGE ACCURACY

8.9599609 VOLTS

1. The measured voltage is always +90% of full scale for the converter used in the system.

Example:	Converter	Voltage
	0–10, ±10	+9.0000
	0–5, ±5	+4.5000
	0–10.24, ±10.24	+9.2160

2. System offsets are automatically removed before the range test is run.
3. The voltage measured in this test is quantized by the A/D and moves in 1 LSB increments as the range is adjusted. The adjustment process should aim for the quantized voltage that is closest to 90% of full scale.
4. During the measurement process for the A/D range, certain corrections are performed by the software to remove amplifier offset errors on the STC and signal processor caused by component aging and temperature drifts. The offset measurements are subtracted from the range reading before printing. Because the offset measurements take place near zero volts, it is possible that systems with unipolar converters will yield offset readings of "OFF SCALE LOW" during this portion of the test. If this happens, the software tries several techniques, including polarity reversal, to make meaningful offset measurements.

   If all of the techniques fail, the message "OFFSET CORRECTION IS OFF SCALE LOW" will be printed. Usually retries will result in successful completion, or the offset can be adjusted in a positive direction in the offset test before running the range test. The range results are not adversely affected by artificially induced offsets.

TEST NO. 5: POWER SUPPLY TEST

In this test, the STC uses three power supply voltages supplied to it (+5, +15 and −15 volts) to produce three voltages that are +90%, +90%, and −90% of full scale for the system A/D converter. These are read by the software, these values are rescaled to represent the actual power supply levels. A typical printout follows:

POWER SUPPLY TEST
+5 V SUPPLY = 5.0008140
+15 V SUPPLY = 14.7547197
−15 V SUPPLY = −15.1123047

This test is also affected by the quantizing levels of the A/D, but they are scaled and do not directly correspond to an LSB value. The power supplies should be set within ±5% of nominal. The +5 volts is produced by a switching supply and has about 70 mV of ripple; thus successive repetitions of this test will show small variations in the +5 volt value. The test will run successfully on unipolar systems since the STC can invert the polarity of the −15 volt signal for measurement by unipolar converters.

TEST NO. 6: SYSTEM NOISE TEST

During this test, the STC produces a stable, quiet voltage of +1/16 full scale. The software then makes 1000 measurements of this value and prints the difference between the highest and lowest values measured, divided by 2, with respect to the A/D input. The number of measurements taken span a time frame that includes a 50 Hz or 60 Hz line frequency cycle; thus, AC power coupling is included as a noise source. The software allows the user to choose gain codes 10, 11, 12 or 13 if the system has a programmable gain signal processor. A typical printout follows:

PEAK-TO-PEAK NOISE TEST
ENTER GAIN CODE 10
PEAK-PEAK NOISE WITH GAIN CODE 12 = +/−0.0024414 V
(REFERENCED TO A/D INPUT)

A few points are worth mentioning here:

1. It is highly unlikely that the voltage being measured will fall directly in the center of an A/D code; thus, very small amounts of noise will cause a 1 LSB change in the A/D output code. Therefore, ±1/2 LSB is the lowest noise to be expected from any system.

2. The noise sources involved in this test include the following:
   A. Self-Test Card noise.
   B. Power supply coupling noise.
   C. Expansion box amplifier and cabling noise (if used).
   D. Signal processor noise.
   E. A/D converter noise.

3. It is important to realize that the measured noise is truly peak-to-peak noise, not 3 sigma or RMS and is being measured on a system with a bandwidth of 1 MHz.

4. The measured noise is always referenced to the A/D input. When measuring noise at signal processor gains greater than unity, the equivalent system input noise is found by dividing the printed result by the signal processor gain.

TEST NO. 7: SLEW RATE TEST

During this test, the ability of the system to accurately follow a fast-moving waveform is checked. Two checks are performed: one for a positive and one for a negative step input. For a bipolar converter, the two voltage levels are located at +90% of full scale (HIGH REF) and −90% of full scale (MINUS REF). For a unipolar converter, the two levels are set at +90% of full scale (HIGH REF) and 1/16 of full scale (LOW REF).

In each case, the testing process is identical. The software addresses the channel that is to be measured, waits a long period of time (approximately 50 μsec), measures and saves the result. The program then addresses the channel that the system will slew from and waits a long period of time. Finally, the original channel is readdressed and measured within the settling time constraints of the system (usually 5 μsec). This value is compared to the previously saved value and the number of counts of difference is printed. Essentially, a comparison is being made between a reading achieved after a long settling time and a reading obtained with a minimum settling time. The minimum settling time allowed is determined solely by the adjustable delay built into the signal processor used in the system, and varies from 5 to 20 μsec, but may be greater in special systems.

A typical printout follows:

SLEW ERROR TEST
ERROR CAUSED BY SLEW FROM MINUS REF TO HIGH REF −00001 COUNTS
ERRORS CAUSED BY SLEW FROM HIGH REF TO MINUS REF 00001 COUNTS

A few points about this test:

1. In the printout, the words "LOW REF" will be substituted for "MINUS REF" for unipolar converters.
2. The word "COUNTS" in the printout is directly equivalent to the number of LSB's of error. Thus, by multiplying the number of counts of error by the voltage value of an LSB in the system under test, the equivalent voltage error can be obtained. The polarity of the number of counts is an indication of undershoot or overshoot. The system is designed to be critically damped, but may have slight undershoot or overshoot.
3. Again, the quantizing effects of the A/D converter mean that very small amounts of slew error can cause 1 LSB errors in the printout. The system timing is generally set so that the unit will settle to ±0.01% of FSR, within the allowable settling time. For a 16-bit, 0-10 volt converter, this would be equivalent to 6-8 counts of error. Increasing the settling time adjustment on the signal processor will decrease the settling time error.

TEST NO. 8: COMMON MODE REJECTION RATIO

During this test, the two analog bus lines (even bus and odd bus) are connected together. These two lines are connected to +90% of full scale and then to −90% of full scale, thus simulating a common-mode voltage applied to shorted inputs. The resulting differential readings are translated into voltages and printed. A sample printout follows:

COMMON MODE REJECTION
CMV = +90% OF FULL SCALE, A/D READING = 0.0048828 VOLTS
CMV = −90% OF FULL SCALE, A/D READING = 0.0000000 VOLTS

NOTES:

1. Because a differential reading is made on shorted inputs, the two readings should be close to zero volts.
2. The quantizing effect of the A/D converter may result in 1 LSB errors even for high common-mode rejection values.
3. Since the readings are near zero it is quite likely that, in unipolar systems, the message "OFF SCALE LOW" may appear. The measure of common mode rejection ratio is the difference between the two readings; thus, in unipolar systems a temporary positive offset of 10–20 mV may be induced by adjusting the signal processor offset potentiometer, using Test No. 3, and then running Test No. 8, readjusting the offset after the test.
4. To calculate the common-mode rejection ratio:

$$CMRR = 20\ LOG_{10} \frac{(+90\%\ RDG) - (-90\%\ RDG)}{2(90\%\ of\ Full\ Scale)}$$

using the sample printout for a ±10 volt 12 bit system.

$$CMRR = 20\ LOG_{10} \frac{(.0048828) - (0)}{2(9)} = 71.3\ dB$$

Note: The CMRR may be higher because only a 1 LSB change was found. RDG = CMV readings.

TEST NO. 9: SIGNAL PROCESSOR GAINS

During this test, the four differential programmable gain codes are tested for offset and gain accuracy. Gain codes 10, 11, 12 and 13 are successively applied. If the system does not have programmable gain, only code 10 is used. A fixed reference voltage of 1/16 full scale is used on all gain codes. A sample printout follows:

MEASUREMENT OF SIGNAL PROCESSOR GAINS
OFFSET WITH GAIN CODE 10 = 0.0000000 V
(REFERENCED TO A/D INPUT)
OFFSET WITH GAIN CODE 11 = 0.0048828 V
(REFERENCED TO A/D INPUT)
OFFSET WITH GAIN CODE 12 = 0.0000000 V
(REFERENCED TO A/D INPUT)
OFFSET WITH GAIN CODE 13 = 0.0000000 V
(REFERENCED TO A/D INPUT)
INPUT VOLTAGE = 0.6250000 VDC
MEASUREMENT WITH GAIN CODE 10 = 0.6250000 V
(REFERENCED TO A/D INPUT)
MEASUREMENT WITH GAIN CODE 11 = 1.2500000 V
(REFERENCED TO A/D INPUT)
MEASUREMENT WITH GAIN CODE 12 = 2.5000000 V
(REFERENCED TO A/D INPUT)
MEASUREMENT WITH GAIN CODE 13 = 5.0000000 V
(REFERENCED TO A/D INPUT)

NOTES:

1. All voltages are given referred to the A/D converter input; thus, signal processor gains are equal to the A/D reading, divided by the input voltage.
2. Again, the quantizing nature of the A/D converter may cause 1 LSB errors for negligible gain errors.
3. Because the offset readings are near zero volts, and because automatic offset correction is used to remove STC offsets during the gain portion of this test, it is likely that in unipolar systems the message "OFF SCALE LOW" may be printed. If this occurs an artificially induced offset may be adjusted into the signal processor using Test No. 3 before running this test. This offset would show up in the offset portion of this test but would not adversely affect the gain readings.

TEST NO. 10: MISSING CODES

This is a fully automatic test where an integrator on the STC, whose direction and speed is under software control, is used to cover the entire input voltage range of the system while a search for each possible bit combination is made at the output of the A/D converter. A sample printout for a 13-bit converter follows:

MISSING CODES TEST
08192 CODES FOUND
00000 CODES MISSING

NOTES:

1. The maximum number of codes possible is 2^N, where N = number of A/D converter bits.
2. Some high resolution converters (14, 15 and 16 bits) may have missing codes and still meet their differential linearity specifications. Check the data sheet for the particular system A/D being tested.
3. The running time for this test is 1-2 minutes, depending on number of bits and voltage range. Test progress may be observed by watching the system front panel. If the system has many (thousands) of missing codes, the running time will be lengthy.

TEST NO. 11: A/D CONVERTER LINEARITY

This test represents an extremely thorough check of A/D converter characteristics for differential linearity, wide codes, narrow codes and missing codes. The test can be run on any binary converter regardless of coding, voltage range or number of bits. The run time of this test is 1-2 minutes, plus printing time for the results.

During the test, a linear, slow-moving ramp is applied to the system input, beginning at minus full scale and going to plus full scale. The speed of the ramp is so slow that it moves much less than one LSB during an A/D conversion. While the ramp is moving up, continuous A/D conversions are made at a constant rate and the memory stores the number of times each code is found. Over 4,000 memory locations are used for data storage. When the test is complete, the software analysis reduces the data, printing a summary of the results. A test of this type is referred to as a histogram.

By observing the results, one can determine the degree of code width variation over the entire range of the A/D, with a resolution of at least 1/60 of an LSB for a 12-bit converter.

The test can be envisioned as shown in Fig. 1.

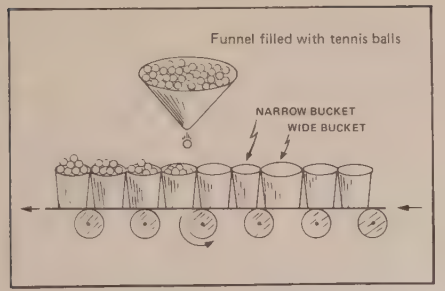

Fig. 1. Pictorial Representation of Code Width Variation Test.

As depicted, a funnel drops tennis balls at a constant rate onto a slowly moving conveyor belt carrying buckets of various sizes. Each tennis ball represents an A/D measurement; each bucket represents one A/D code (for a 12-bit converter, there would be over 4,000 buckets). The conveyor belt moves at a constant speed, representing the integrator ramp which changes at a constant rate.

When all the buckets have passed under the funnel, the relative sizes of the buckets may be measured by counting the number of balls in each one. A list is then made, giving each bucket a number and tabulating the number of balls in each bucket. By scanning this list, one can pick out the narrowest and widest buckets to determine the amount by which the bucket sizes vary.

Unfortunately, the list would have over 4,000 entries, would take a long time to print, and a long time to interpret. However, one could reduce the data by listing the number of balls in the widest buckets, the number of balls in the narrowest buckets and the number of buckets containing the in-between numbers of balls. This technique will shorten the list, while maintaining the integrity of the data.

If there were 1,000 buckets, the list might appear as shown in Table 1.

NO. OF BALLS	NO. OF BUCKETS	
105	1	WIDEST BUCKET
104	3	
103	7	
102	75	
101	194	
100	500	
99	125	
98	74	
97	19	
96	1	
95	1	NARROWEST BUCKET
0	0	MISSING BUCKETS

Table 1. Tennis Ball Population In Buckets

The above list shows that one bucket has 105 balls in it, three buckets have 104 balls in them, seven buckets have 103 balls in them, etc. Note that most of the buckets have 100 balls in them, the widest bucket has 105 balls, and the narrowest bucket has 95 balls in it. Thus, the maximum deviation in bucket size is ±5% from the average. In addition, since the average bucket has 100 balls in it, the test resolution is 1% of a bucket. Furthermore, if the "No. of Buckets" column is summed, 1,000 is obtained for a result, thus showing that all of the buckets have been accounted for. This is also indicated by the last entry in the list which says that no buckets have no balls in them i.e., there were no missing buckets.

A sample printout for a 12-bit A/D system, listed in Table 2, will now be examined.

NO. OF TIMES FOUND	NO. OF CODES		NO. OF TIMES FOUND	NO. OF CODES	
00093	00001	WIDEST CODE	00061	00197	
00092	00000		00060	00202	
00091	00001		00059	00191	
00090	00001		00058	00210	
00089	00001		00057	00165	
00088	00003		00056	00146	
00087	00000		00055	00142	
00086	00001		00054	00114	
00085	00004		00053	00102	
00084	00001		00052	00076	
00083	00005		00051	00078	
00082	00010		00050	00047	
00081	00010		00049	00047	
00080	00015		00048	00042	
00079	00025		00047	00027	
00078	00019		00046	00019	
00077	00043		00045	00017	
00076	00050		00044	00006	
00075	00073		00043	00008	
00074	00087		00042	00002	
00073	00097		00041	00004	
00072	00107		00040	00004	
00071	00123		00039	00002	
00070	00118		00038	00000	
00069	00135		00037	00000	
00068	00171		00036	00000	
00067	00162		00035	00000	
00066	00190		00034	00000	
00065	00191		00033	00000	
00064	00200		00032	00000	
00063	00196		00031	00001	NARROWEST CODE
00062	00205		00000	00000	MISSING CODES

Table 2. Linearity Test of A/D Converter.

Here it is seen that the widest code was found 93 times, the narrowest code 31 times, and most codes were found about 62 times. Thus the maximum and minimum code width deviations are ±50% from nominal. A tolerance of ±1/2 LSB code width deviation is normal for a 12-bit A/D converter. The last entry in the column indicates that there were no missing codes. If the numbers in the code column are summed, the result is 4,094. A 12-bit converter has 4,096 possible codes, but since code widths are being measured, the program ignores the top and bottom codes since they have only one edge i.e., their width cannot be measured. Note also that the test resolution is 1/60 of an LSB.

The appearance of the printout will vary with different resolution and voltage range converters. The printout will always begin with the widest code and will proceed in numerical sequence down the "No. of Times Found" column, until the narrowest code is listed. The last entry will indicate how many codes were missing.

It is not necessary to sum the numbers in the code column, since they will always total correctly. The total for an 8-bit converter would be 254; 1,022 for a 10-bit converter; and 4,094 for a 12-bit converter. To avoid using more than 4 K of memory for data storage, converters with a resolution greater than 12 bits are treated as 12-bit converters in this test. Thus 13, 14, 15 and 16-bit units will also have 4,094 codes tested. It is noteworthy that the resolution of the test will support 16-bit converters, even though they are tested on a 12-bit level. For example, if the printout shows that all codes are within ±1/8 LSB on a 12-bit level, this would correspond to ±1/2 LSB on a 14-bit level.

TEST NO. 12: CODE CENTERS

In this test, the user may request any octal code that the A/D converter is capable of producing and the program will manipulate the integrator in the STC to produce a voltage that corresponds to the center of the requested code. The voltage can be read with a precision DVM and compared to the ideal voltage. This voltage is available at the rear of the STC on pins N (analog ground) and M (integrator output). A sample entry for a 0-5 converter follows:

```
CODE CENTER
ENTER VALUE FOR CODE CENTER 120000
DESIRED VALUE = 3.1250000
```

The operator must enter a 6-digit octal number, left-hand justified, for the code center value and he may not ask for the absolute top or bottom converter codes. These two codes have only one edge; thus, their centers cannot be measured. The program calculates the ideal voltage value and prints it for comparison with the measured voltage.

The program then enters an endless loop where it maintains the integrator voltage at the desired code center. The requested code will be displayed on the A/D converter data lights during the test. This test is ideal for checking offset and range calibration to a high precision, and testing converter linearity over large voltage changes.

Since this is an active feedback loop, changes in the offset and range controls can be made while the program is running, and the results will be continually displayed on the DVM. Further information on this technique is available in a technical reprint of an Analogic article entitled "CATCH MISSING CODES". Type "CTRL C" any time to abort the test.

TEST NO. 13: PASS/FAIL LIGHTS

This is a visual test of the red and green lights mounted toward the rear of the STC. The lights are cycled once through the pattern below, waiting about five seconds at each step.

1. Green on.
2. Red on.
3. Both on.
4. Both off.

TEST NO. 14: EXTERNAL DIGITAL OUTPUT TEST

This test allows the user to program the state of the eight external digital outputs on the pins available at the rear of the STC. The user types either a "1" or a "0" for each signal DØ through D7. DØ corresponds to pin 14 (pin name DYØ) on the STC.

Sample printout:

```
EXTERNAL DIGITAL OUTPUT TEST

DØ = Ø
D1 = 1
D2 = 1
D3 = Ø
D4 = 1
D5 = 1
D6 = Ø
D7 = 1
CODE TRANSMITTED
```

TEST NO. 15: EXTERNAL DIGITAL INPUT TEST

This test reads the state of the eight external digital inputs that can be supplied to the rear pins on the STC. The state of each input is listed in terms of "1" or "0". If no signals are connected to the input pins, they will be read as 1's. Signal DØ corresponds to DXØ, pin R, on the STC.

```
EXTERNAL DIGITAL INPUT TEST

DØ = 1
D1 = 1
D2 = Ø
D3 = Ø
D4 = Ø
D5 = 1
D6 = Ø
D7 = 1
```

TEST NO. 16: EXTERNAL ANALOG INPUTS

In this test, the A/D converter and signal processor are used to read the eight external differential analog input channels available at the rear of the STC. The user may request any gain code 10, 11, 12 or 13, if the system has programmable gain. CHØ, as printed, corresponds to CHØ on the STC, denoted by signals ANØ on pin C (HI side) and AIØ on pin 3 (LO side).

```
EXTERNAL ANALOG INPUTS
ENTER GAIN CODE 10

CH 0  = -8.5986328 V (REFERENCED TO A/D INPUT)
CH 2  = -7.9833984 V (REFERENCED TO A/D INPUT)
CH 4  = -8.5986328 V (REFERENCED TO A/D INPUT)
CH 6  = -9.2382812 V (REFERENCED TO A/D INPUT)
CH 10 =  3.9990234 V (REFERENCED TO A/D INPUT)
CH 12 =  3.8183594 V (REFERENCED TO A/D INPUT)
CH 14 = -4.9072266 V (REFERENCED TO A/D INPUT)
CH 16 = -7.3828125 V (REFERENCED TO A/D INPUT)
```

ANALOGIC.■

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Tel. (44) 932-41251 ■ Telex 851-928030
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Cincinnati, Ohio (606) 371-0064 ■ San Jose, Calif. (408) 247-6401
Tustin, Calif. (714) 838-7243 ■ Garland, Texas (214) 681-0483
Houston, Texas (713) 777-6360

AVAILABLE FROM:

Bulletin No. 16-100129 REV 1

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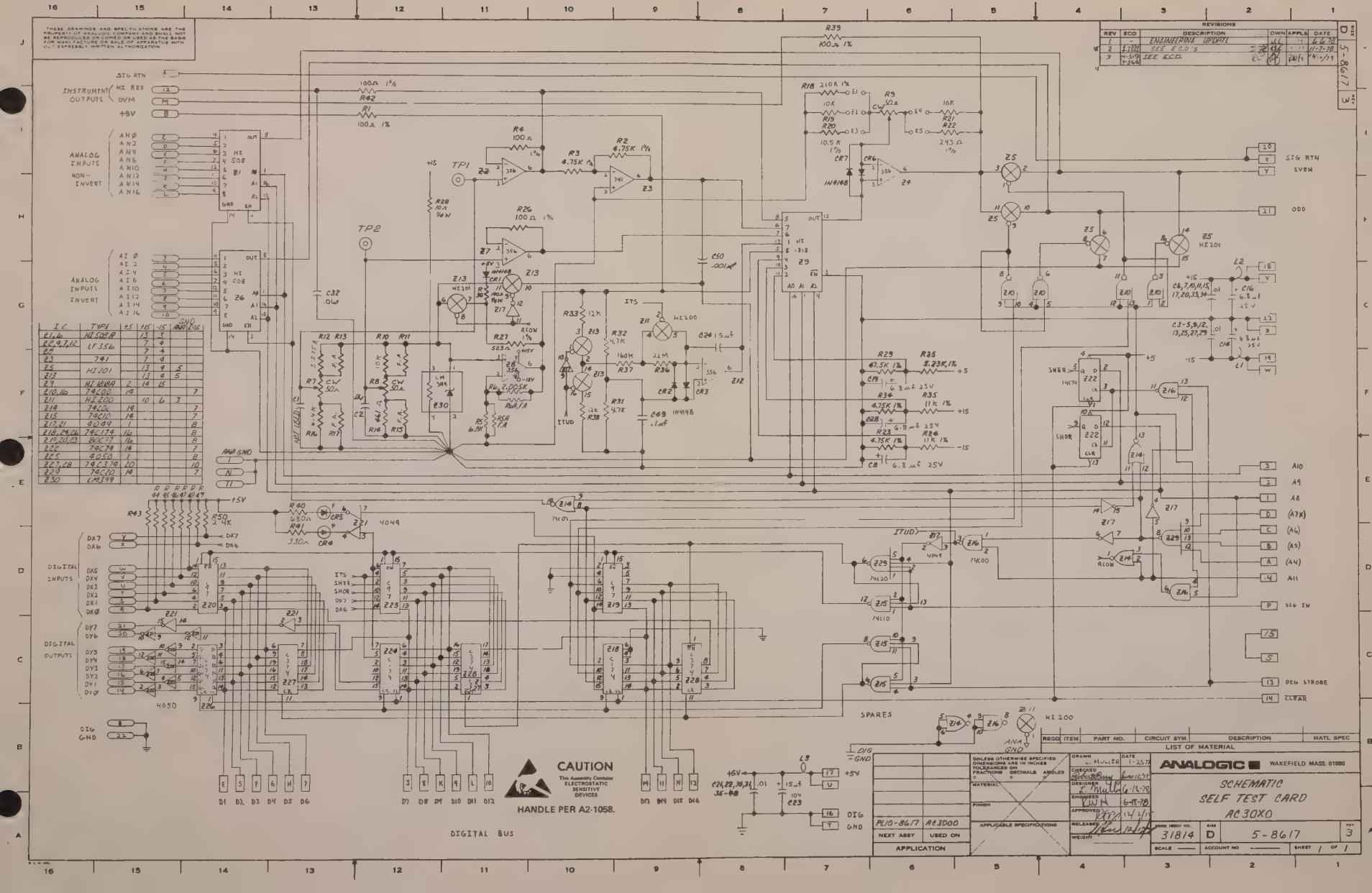
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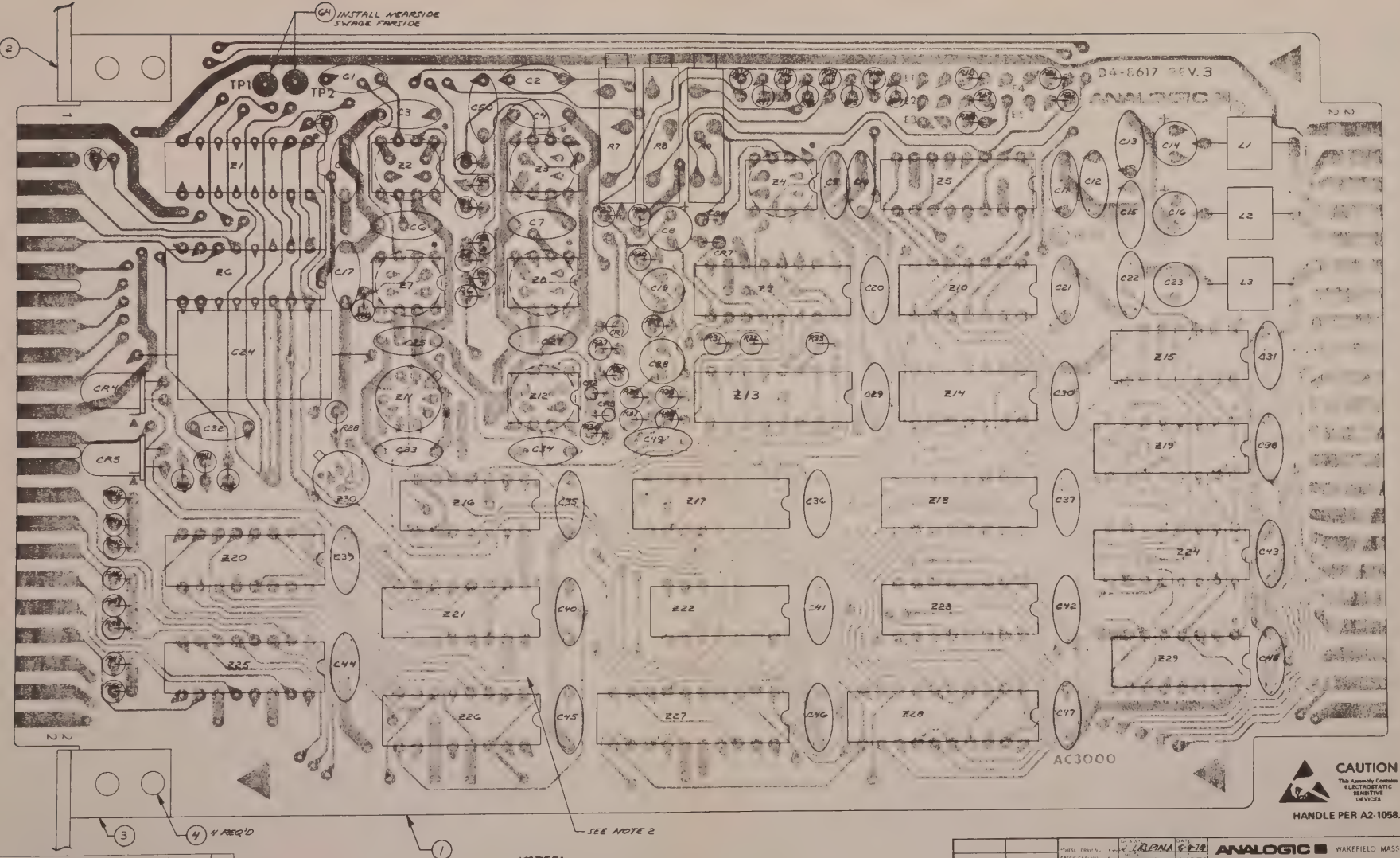
REVISIONS
REV ECO DESCRIPTION DWN APPD DATE
1 — ENGINEERING UPDATE
2 4-2398 SEE ECO'S
3 4-5197 4-5660 SEE ECO.
5-8617
SIG RTN
INSTRUMENT OUTPUTS
HI REF
DVM
+9V
ANALOG INPUTS NON-INVERT
ANALOG INPUTS INVERT
TP1
TP2
+15
-15
+5
-5
C32 .01uf
C50 .001uf
C69 .1uf
C24,28,30,31 .01
C23 15.uf
L3
R39 100Ω 1%
R18 210K 1%
R19 10K
R20 10.5K 1%
R9 50Ω
R21 10K
R22 243Ω 1%
R4 100Ω 1%
R3 4.75K 1%
R2 4.75K 1%
R26 100Ω 1%
R28 10Ω 1/4W
R27 523Ω 1%
R6 2.005K 1%
R5 6.8K
R33 12K
R32 4.7K
R37 160K
R36 22M
R31 4.7K
R38 12K
R29 47.5K 1%
R35 5.23K 1%
R34 4.75K 1%
R23 4.75K 1%
R24 11K 1%
C79 6.8mf 25V
C28 6.8mf 25V
C8 6.8mf 25V
C16 6.8mf 25V
C18 6.8mf 25V
C6,7,10,11,15,17,20,33,34 .01
C2-5,9,12,13,25,27,29 .01
R43 R50 2.4K
R49 680Ω
R41 330Ω
IN4148
IN4148
HI201
HI200
HI508A
HI-508
LF356
741
HI-318
HI-201
HI-200
74C04
74C10
4049
74C74
4050
74C374
74C00
74C30
LM 399
4030
DIGITAL INPUTS
DIGITAL OUTPUTS
DIG GND
ANA GND
SPARES
DIGITAL BUS
SIG RTN EVEN
ODD
A10
A9
A8
(A7X)
(A6)
(A5)
(A4)
A11
DIG IN
DIG STROBE
CLEAR
CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.
REQD ITEM PART NO. CIRCUIT SYM DESCRIPTION MATL SPEC
LIST OF MATERIAL
PL10-8617 A03D00
NEXT ASSY USED ON
APPLICATION
DRAWN L. MULLER 1-3-79
CHECKED 1-15-79
DESIGNER L. Mullen 1-15-79
ENGINEER 6-11-79
APPROVED 4/15/79
RELEASED
WEIGHT
ANALOGIC WAKEFIELD MASS. 01880
SCHEMATIC
SELF TEST CARD
AC30X0
DRWG IDENT NO. 31814
SIZE D
5-8617
REV 3
SCALE
ACCOUNT NO
SHEET 1 OF 1



REVISIONS					
REV.	ECO	DESCRIPTION	DWN	APPLS	DATE
D	8717 & 326	SEE ECO	RP	RBS Pump	4/4/79

7-8617 REV 3

CR5 (REF)

SECTION 'A-A'

NOTES:
1. FOR SCHEMATIC SEE D5-8617
2. DOT INDICATES PIN #1 OF I.C.'S
3. ASSEMBLY PER A2-1027

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			CHECKED R. PERRY 6-15-78	ASSEMBLY SELF TEST CARD AC30X0	
			ENGR L. MULLER 6-8-78		
			PROD ENGR E. HAVOUKE 6-14-78		
			APPROVED		
REV 0-8617	AC3000		RELEASED S. LEE 12/27/78		
NEXT ASSY	USED ON		WEIGHT	SIZE IDENT NO 31814	DWG D 7-8617 REV 3
APPLICATION				SCALE 4:1	ACCOUNT NO. SHEET 1 OF 1

15
I/O Cable Assemblies

Card Number	Drawing Number	Title
—	C6-3180	Terminal Barrier Strip Mechanical Outline
—	D7-1590	Cable Assembly (CA-SE-10)
—	D7-1582	Cable Assembly (CA-DI-10)
—	D7-1583	Cable Assembly (CA-DA-10)
—	D7-1581	Cable Assembly (CA-DR-10)
—	D7-2301	Cable Assembly (CA-IS-10)
—	—	Cable Assembly (CA-SH-10)

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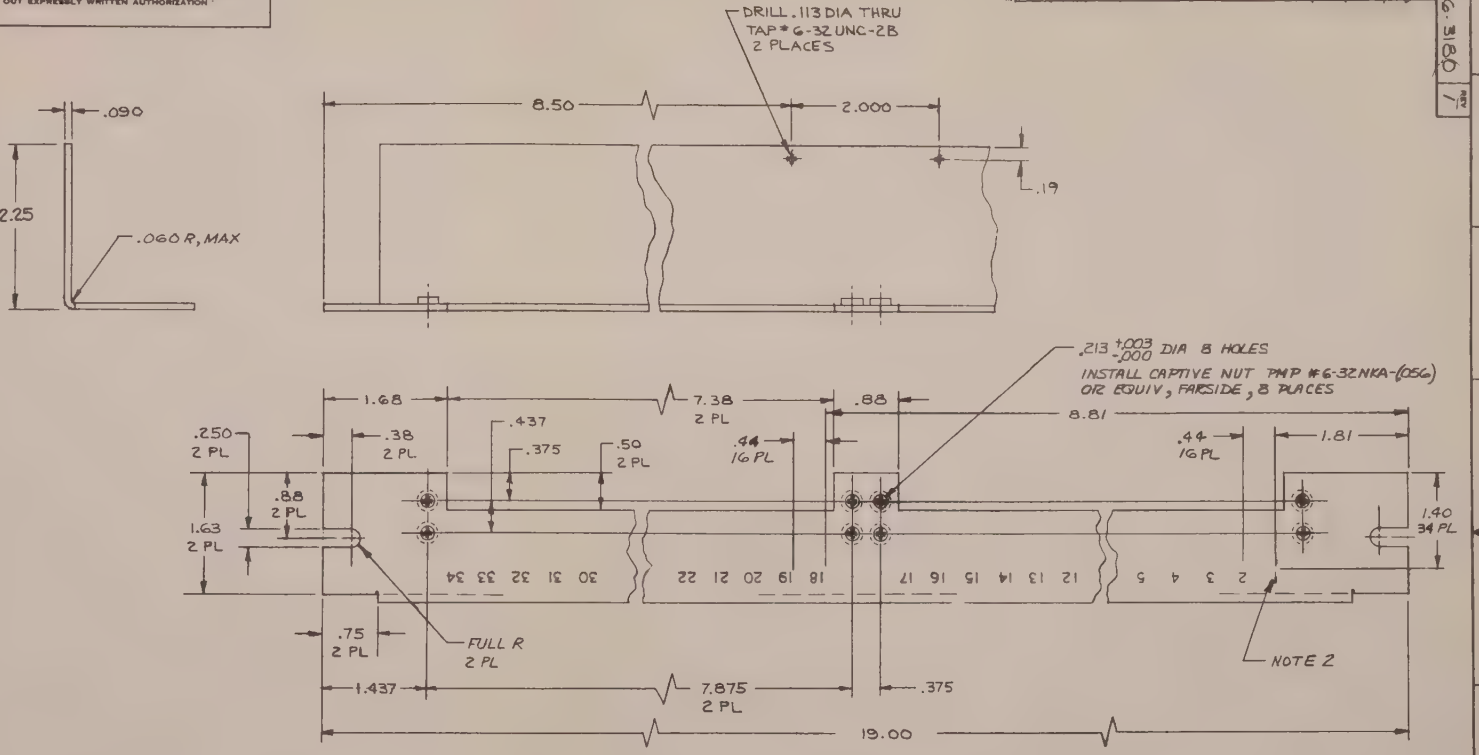
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPD	DATE
1	4012A	SEE ECO	RB	SJ	8 May 78

SIZE C | 6-3180 | REV 1



NOTES:

1. FINISH: MASK THREADS, PRIME & PAINT BLACK ENAMEL, SEMI-GLOSS/FED-STD-595 COLOR CHIP NO. 27038.
2. SILKSCREEN .12 HIGH WHITE CHARACTERS (1 THRU 34) (ACCEPTABLE ALTERNATE: SINGLE ADHESIVE BACKED LABEL: BLACK BACKGROUND WITH WHITE OR SILVER LETTERS).

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC
				LIST OF MATERIAL	

PL10-2159	ANS400
PL10-2158	ANS400
PL10-2157	ANS400
PL10-2156	ANS400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS ANGLES
XX ± .03 XXX ± .010 ± —
MATERIAL .030 THK 3052-H32 AL
FINISH NOTE 1
APPLICABLE SPECIFICATIONS

DRAWN	M Carter	DATE 2-17-77
CHECKED	[illegible]	2-18-77
DESIGNER	R Durain	18 FEB 77
ENGINEER	[illegible]	2-18-77
APPROVED	[illegible]	2-18-77
RELEASED	[illegible]	2/18/77
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

MOUNT, TERMINAL BOARD

CODE IDENT NO	SIZE		REV
31814	C	6-3180	1
SCALE 1/1	ACCOUNT NO		SHEET 1 OF 1

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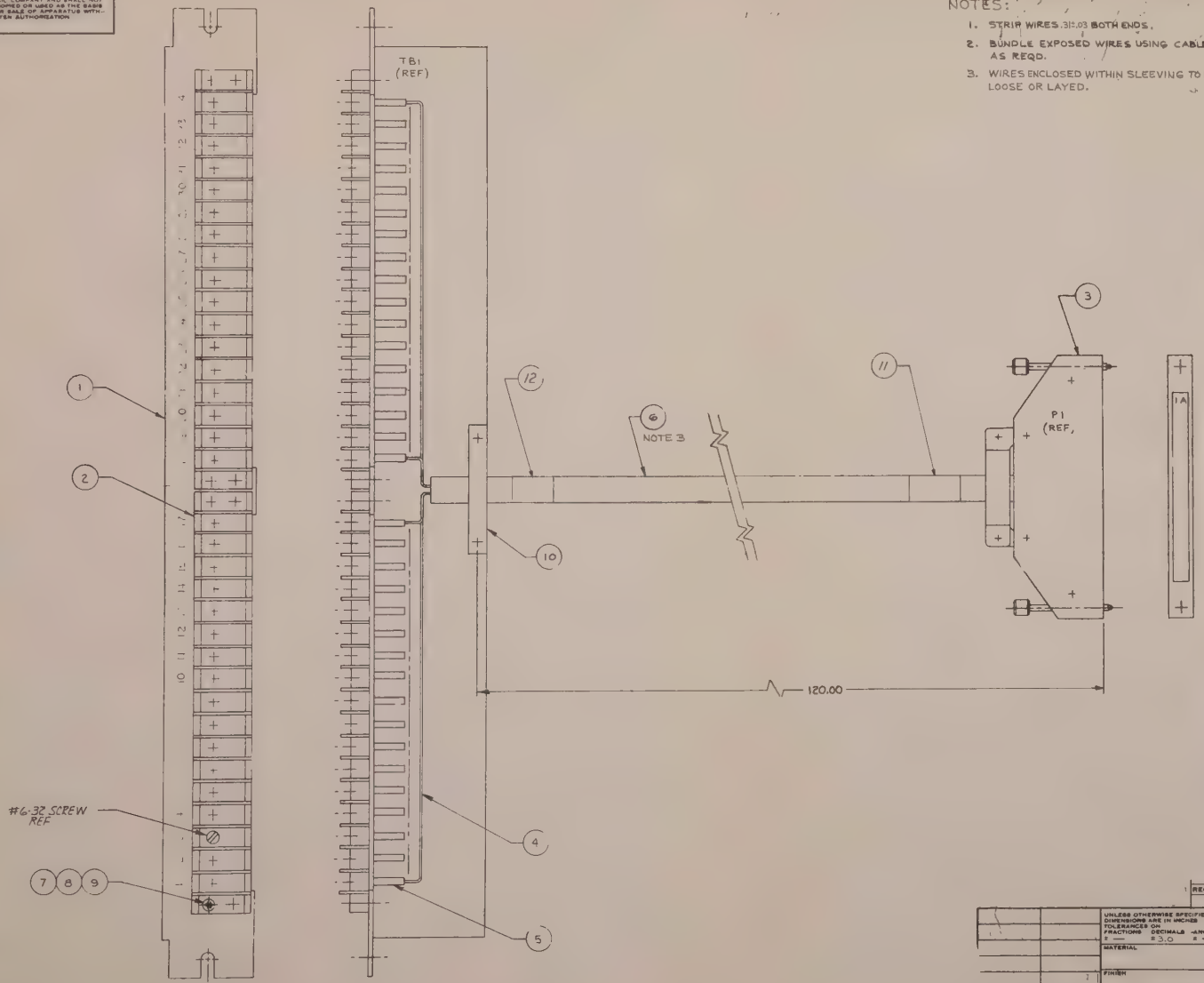
NOTES:

1. STRIP WIRES .31±.03 BOTH ENDS.
2. BUNDLE EXPOSED WIRES USING CABLE TIES. AS REQD.
3. WIRES ENCLOSED WITHIN SLEEVING TO BE LOOSE OR LAYED.

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPR	DATE
1	A-0041	ADDED ITEMS 11 & 12	GA	WR	6-30-77
2	A-0048	SEE ECO	GA/DZ	RC	7-26-77



WIRING TABLE

ITEM NO.	WIRE NO.	SIZE AWG	COLOR	FROM	TO	SIGNAL NAME
4	1	24	WHITE	TB1-1	P1-C	CHAN 1
	2			TB1-2	P1-3	2
	3			TB1-3	P1-D	3
	4			TB1-4	P1-4	4
	5			TB1-5	P1-E	5
	6			TB1-6	P1-5	6
	7			TB1-7	P1-F	7
	8			TB1-8	P1-6	8
	9			TB1-9	P1-H	9
	10			TB1-10	P1-7	10
	11			TB1-11	P1-J	11
	12			TB1-12	P1-8	12
	13			TB1-13	P1-L	13
	14			TB1-14	P1-10	14
	15			TB1-15	P1-M	15
	16			TB1-16	P1-11	CHAN 16
	17			TB1-17	P1-E	ANALOG GND
	18			TB1-18	P1-22	SIGNAL RTN
	19			TB1-19	P1-N	CHAN 17
	20			TB1-20	P1-12	18
	21			TB1-21	P1-P	19
	22			TB1-22	P1-13	20
	23			TB1-23	P1-S	21
	24			TB1-24	P1-15	22
	25			TB1-25	P1-T	23
	26			TB1-26	P1-16	24
	27			TB1-27	P1-U	25
	28			TB1-28	P1-17	26
	29			TB1-29	P1-V	27
	30			TB1-30	P1-18	28
	31			TB1-31	P1-W	29
	32			TB1-32	P1-19	30
	33			TB1-33	P1-X	31
	34			TB1-34	P1-20	CHAN 32
	35			P1-22	P1-A	SIGNAL RTN
	36			P1-2	P1-B	ANALOG GND
	37			P1-9	P1-K	
	38			P1-14	P1-R	
	39			P1-21	P1-Y	
	40			P1-Y	P1-R	
	41			P1-14	P1-9	
4	42	24	WHITE	P1-K	P1-B	ANALOG GND

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES ± 3.0 ±	DRAWN	W.H. Carter	DATE 2-28-77
	CHECKED		3-4-77
MATERIAL	DESIGNER		3-9-77
FINISH	ENGINEER		
	APPROVED		
APPLICABLE SPECIFICATIONS	RELEASED		
	WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

CABLE ASSEMBLY
(CA-SE-10)

PL10-2160	AN5400	31814	D 7-1590
NEXT ASSY	USED ON	SCALE 1/1	ACCOUNT NO.
APPLICATION			SHEET 1

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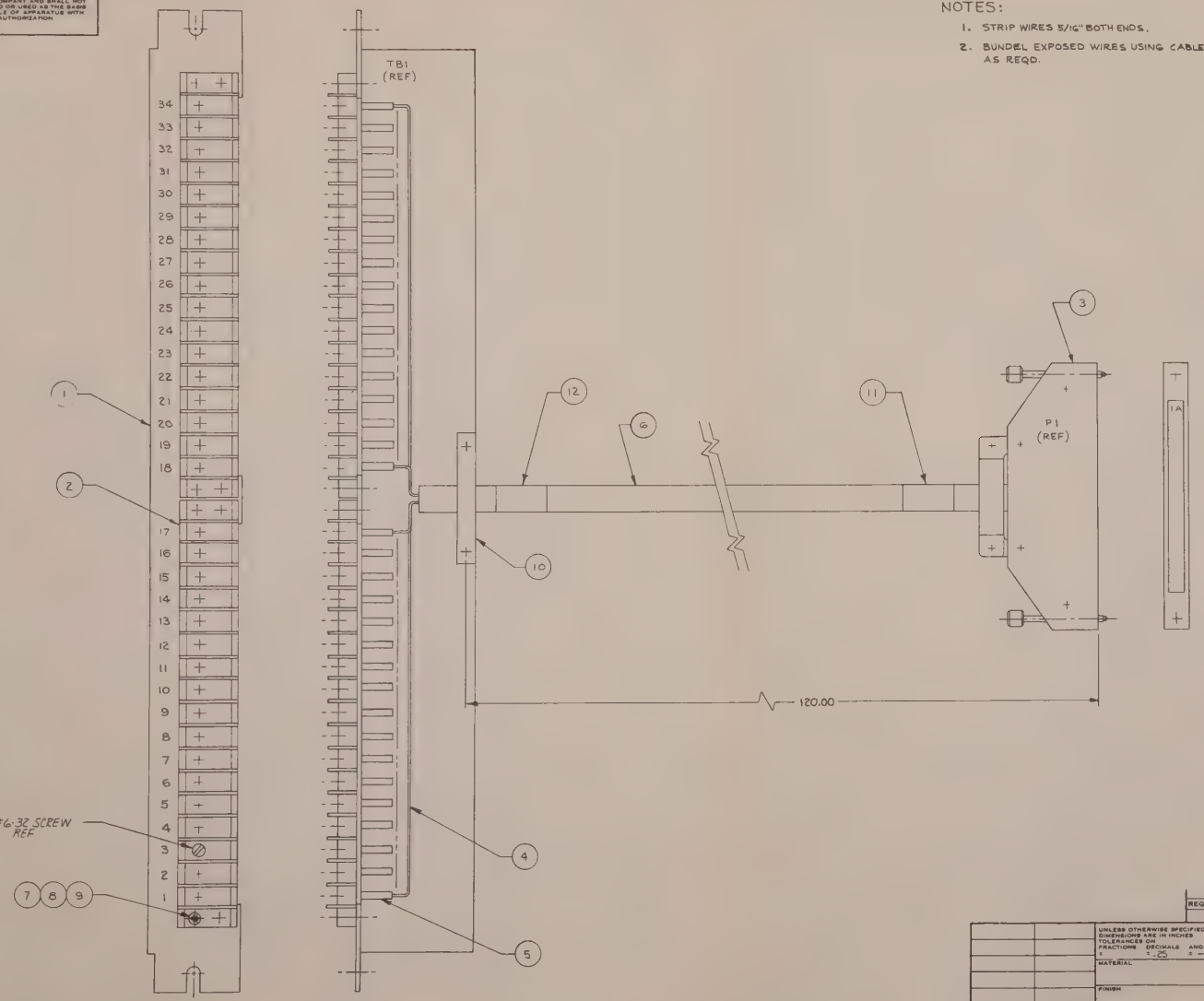
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPR'D	DATE
1	4004	SEE E.C.O.	RF	JSC	6-30-77

D 7-1582 1

NOTES:

1. STRIP WIRES 5/16" BOTH ENDS.
2. BUNDEL EXPOSED WIRES USING CABLE TIES AS REQD.



WIRING TABLE

ITEM NO.	WIRE NO.	SIZE AWG	COLOR	FROM	TO	SIGNAL NAME	
4	1	24	WHITE	TB1-1	P1-C	HI } CHAN 1	TWIST
	2			TB1-2	P1-3	LO }	
	3			TB1-3	P1-D	HI } CHAN 2	
	4			TB1-4	P1-4	LO }	
	5			TB1-5	P1-E	HI } CHAN 3	
	6			TB1-6	P1-5	LO }	
	7			TB1-7	P1-F	HI } CHAN 4	
	8			TB1-8	P1-6	LO }	
	9			TB1-9	P1-H	HI } CHAN 5	
	10			TB1-10	P1-7	LO }	
	11			TB1-11	P1-J	HI } CHAN 6	
	12			TB1-12	P1-8	LO }	
	13			TB1-13	P1-L	HI } CHAN 7	
	14			TB1-14	P1-10	LO }	
	15			TB1-15	P1-M	HI } CHAN 8	TWIST
	16			TB1-16	P1-11	LO }	
	17			TB1-17	P1-2	ANALOG GND	
	18			TB1-18	P1-22	SIGNAL RTN	
	19			TB1-19	P1-N	HI } CHAN 9	TWIST
	20			TB1-20	P1-12	LO }	
	21			TB1-21	P1-P	HI } CHAN 10	
	22			TB1-22	P1-13	LO }	
	23			TB1-23	P1-S	HI } CHAN 11	
	24			TB1-24	P1-15	LO }	
	25			TB1-25	P1-T	HI } CHAN 12	
	26			TB1-26	P1-16	LO }	
	27			TB1-27	P1-U	HI } CHAN 13	
	28			TB1-28	P1-17	LO }	
	29			TB1-29	P1-V	HI } CHAN 14	
	30			TB1-30	P1-18	LO }	
	31			TB1-31	P1-W	HI } CHAN 15	
	32			TB1-32	P1-19	LO }	
	33			TB1-33	P1-X	HI } CHAN 16	TWIST
	34			TB1-34	P1-20	LO }	
	35			P1-22	P1-A	SIGNAL RTN	
	36			P1-2	P1-B	ANALOG GND	
	37			P1-9	P1-K		
	38			P1-14	P1-R		
	39			P1-21	P1-Y		
	40			P1-Y	P1-R		
	41			P1-14	P1-9		
4	42	24	WHITE	P1-K	P1-B	ANALOG GND	

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PL10-Z158	ANS400		
NEXT ASSY	USED ON		
APPLICATION			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS ± DECIMALS ± .05 ANGLES ± —
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

DRAWN	M.W. Carter	DATE 1/3/77
CHECKED	Robert Hunter	1/6/77
DESIGNER	R. Hunter	1 FEB 77
ENGINEER	L.W. Williams	2-15-77
APPROVED	M. J. Bowman	2-17-77
RELEASED	C. Meehan	2-18-77
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

CABLE ASSEMBLY
(CA-DI-10)

CODE IDENT NO	SIZE	DWG NO	REV
31814	D	7-1582	1
SCALE 1/1	ACCOUNT NO.	SHEET 1	OF 1

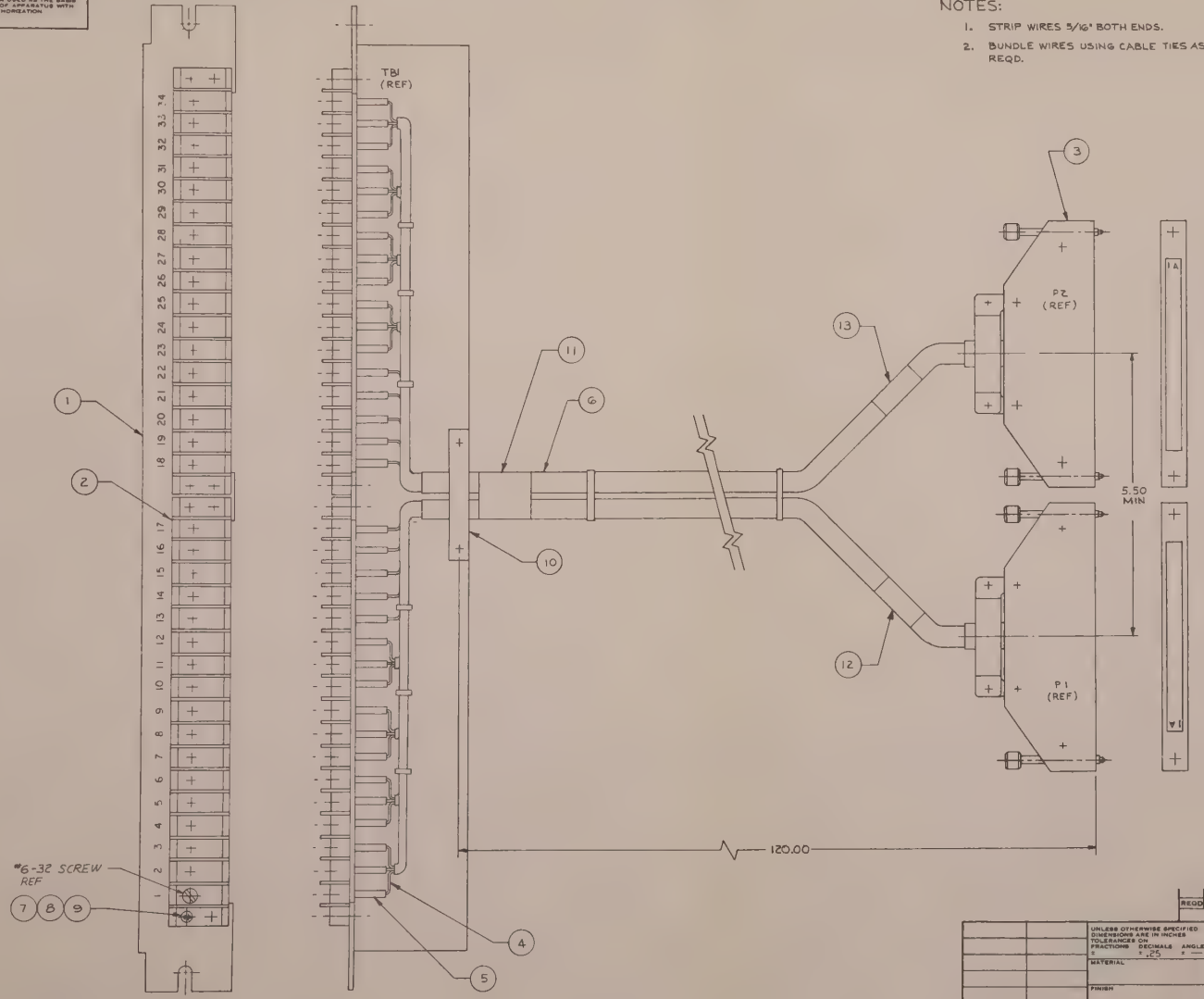
THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF ANALOGIC COMPANY AND SHALL NOT BE REPRODUCED OR COPIED OR USED AS THE BASIS FOR MANUFACTURE OR SALE OF APPARATUS WITH OUT EXPRESSELY WRITTEN AUTHORIZATION

NOTES:

1. STRIP WIRES 5/16" BOTH ENDS.
2. BUNDLE WIRES USING CABLE TIES AS REQD.

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPD	DATE
1	A-0041	SEE E.C.O.	LM	LM	6 SEP 77
2	A-0238	SEE ECO	LM	LM	28 DEC 77

DSE 7-1583 REV 2



WIRING TABLE

ITEM NO.	WIRE NO.	SIZE AWG	COLOR	FROM	TO	SIGNAL NAME	
4	1	24	WHITE	TBI-1	P1-D	OUT Ø	CARD 1
	2			TBI-2	P1-E	RTN Ø	
	3			TBI-3	P1-5	SENSE Ø	
	4			TBI-4	P1-J	OUT 1	
	5			TBI-5	P1-K	RTN 1	
	6			TBI-6	P1-9	SENSE 1	
	7			TBI-7	P1-P	OUT 2	
	8			TBI-8	P1-R	RTN 2	
	9			TBI-9	P1-4	SENSE 2	
	10			TBI-10	P1-J	OUT 3	
	11			TBI-11	P1-V	RTN 3	
	12			TBI-12	P1-18	SENSE 3	
	13			TBI-13	P1-4	LOAD Ø	
	14			TBI-14	P1-6	SPARE	
	15			TBI-15	P1-21	DIG. GND	
	16			TBI-16	P1-Z	ANA. GND	
	17			TBI-17	P1-1	ANA. GND	
	18			TBI-18	P2-D	OUT Ø	CARD 2
	19			TBI-19	P2-E	RTN Ø	
	20			TBI-20	P2-5	SENSE Ø	
	21			TBI-21	P2-J	OUT 1	
	22			TBI-22	P2-K	RTN 1	
	23			TBI-23	P2-9	SENSE 1	
	24			TBI-24	P2-P	OUT 2	
	25			TBI-25	P2-R	RTN 2	
	26			TBI-26	P2-14	SENSE 2	
	27			TBI-27	P2-U	OUT 3	
	28			TBI-28	P2-V	RTN 3	
	29			TBI-29	P2-18	SENSE 3	
	30			TBI-30	P2-4	LOAD Ø	
	31			TBI-31	P2-8	SPARE	
	32			TBI-32	P2-21	DIG. GND	
	33			TBI-33	P2-Z	ANA. GND	
4	34	24	WHITE	TBI-34	P2-1	ANA. GND	

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PL10-2159	AN 5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± .25 DECIMALS ± — ANGLES ± —

MATERIAL

FINISH

APPLICABLE SPECIFICATIONS

DRAWN	Phil Carter	1/1/77
CHECKED	John Combs	1/21/77
DESIGNER	[illegible]	1 FEB 77
ENGINEER	[illegible]	2-3-77
APPROVED	H. J. Jarvis	2-18-77
RELEASED	[illegible]	3 MAR 77
WEIGHT		

ANALOGIC WAKEFIELD, MASS 01880

CABLE ASSEMBLY (CA-DA-10)

CODE IDENT NO.	DSE	REV
31814	D 7-1583	2

SCALE 1/1 ACCOUNT NO. SHEET 1 OF 1

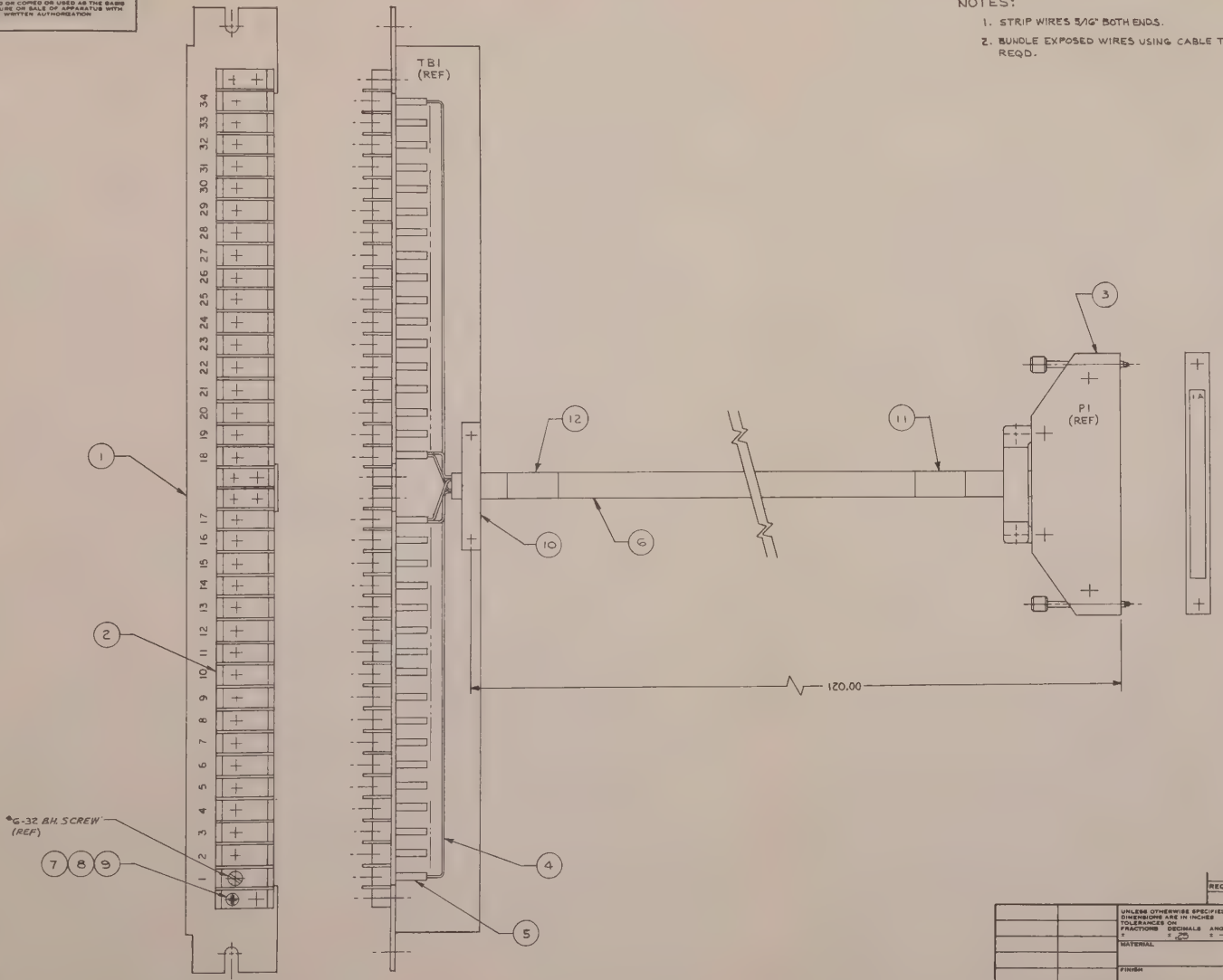
THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF ANALOGIC COMPANY AND SHALL NOT BE REPRODUCED OR COPIED OR USED AS THE BASIS FOR MANUFACTURE OR SALE OF APPARATUS WITHOUT EXPRESSLY WRITTEN AUTHORIZATION

NOTES:

1. STRIP WIRES 3/16" BOTH ENDS.
2. BUNDLE EXPOSED WIRES USING CABLE TIES AS REQD.

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APP'D	DATE
1	4-0041	SEE E.C.O.			
M 2	H-0238	SEE ECO			

D 7-1581 2



WIRING TABLE

ITEM NO.	WIRE NO.	SIZE AWG	COLOR	FROM	TO	SIGNAL NAME
4	1	24	WHITE	TB1-1	P1-19	B16
	2			TB1-2	P1-18	B15
	3			TB1-3	P1-17	B14
	4			TB1-4	P1-16	B13
	5			TB1-5	P1-15	B12
	6			TB1-6	P1-14	B11
	7			TB1-7	P1-13	B10
	8			TB1-8	P1-12	B9
	9			TB1-9	P1-11	B8
	10			TB1-10	P1-10	B7
	11			TB1-11	P1-9	B6
	12			TB1-12	P1-8	B5
	13			TB1-13	P1 7	B4
	14			TB1-14	P1 6	B3
	15			TB1-15	P1-5	B2
	16			TB1-16	P1-4	B1
	17			TB1-17	P1 2	PWR 1
	18			P1-2	P1 3	PWR 1
	19			P1-C	P1-3	PWR 1
	20			P1-C	P1 22	PWR 1
	21			P1-22	P1-21	PWR 1
	22			TB1-19	P1-W	B16
	23			TB1-20	P1-V	B15
	24			TB1-21	P1-U	B14
	25			TB1-22	P1-T	B13
	26			TB1-23	P1-S	B12
	27			TB1-24	P1-R	B11
	28			TB1-25	P1-P	B10
	29			TB1-26	P1-N	B9
	30			TB1-27	P1-M	B8
	31			TB1-28	P1-L	B7
	32			TB1-29	P-K	B6
	33			TB1-30	P-J	B5
	34			TB1-31	P1-H	B4
	35			TB1-32	P1-F	B3
	36			TB1-33	P1-E	B2
	37			TB1-34	P1-D	B1
	38			TB1-18	P1-Z	PWR 2
	39			P1-Z	P1-Y	PWR 2
4	40	24	WHITE	P1-Y	P1-B	PWR 2

PORT A

PORT B

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PLIO-2157	AN5400		
NEXT ASSY	USED ON		
APPLICATION			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

DRAWN		DATE 1/10/77
CHECKED		1/22/77
ENGINEER		2-8-77
ENGINEER		2-15-77
APPROVED		3-18-77
RELEASED		3-9-77
WEIGHT		

ANALOGIC WAKEFIELD, MASS 01880

CABLE ASSEMBLY
(CA-DR-10)

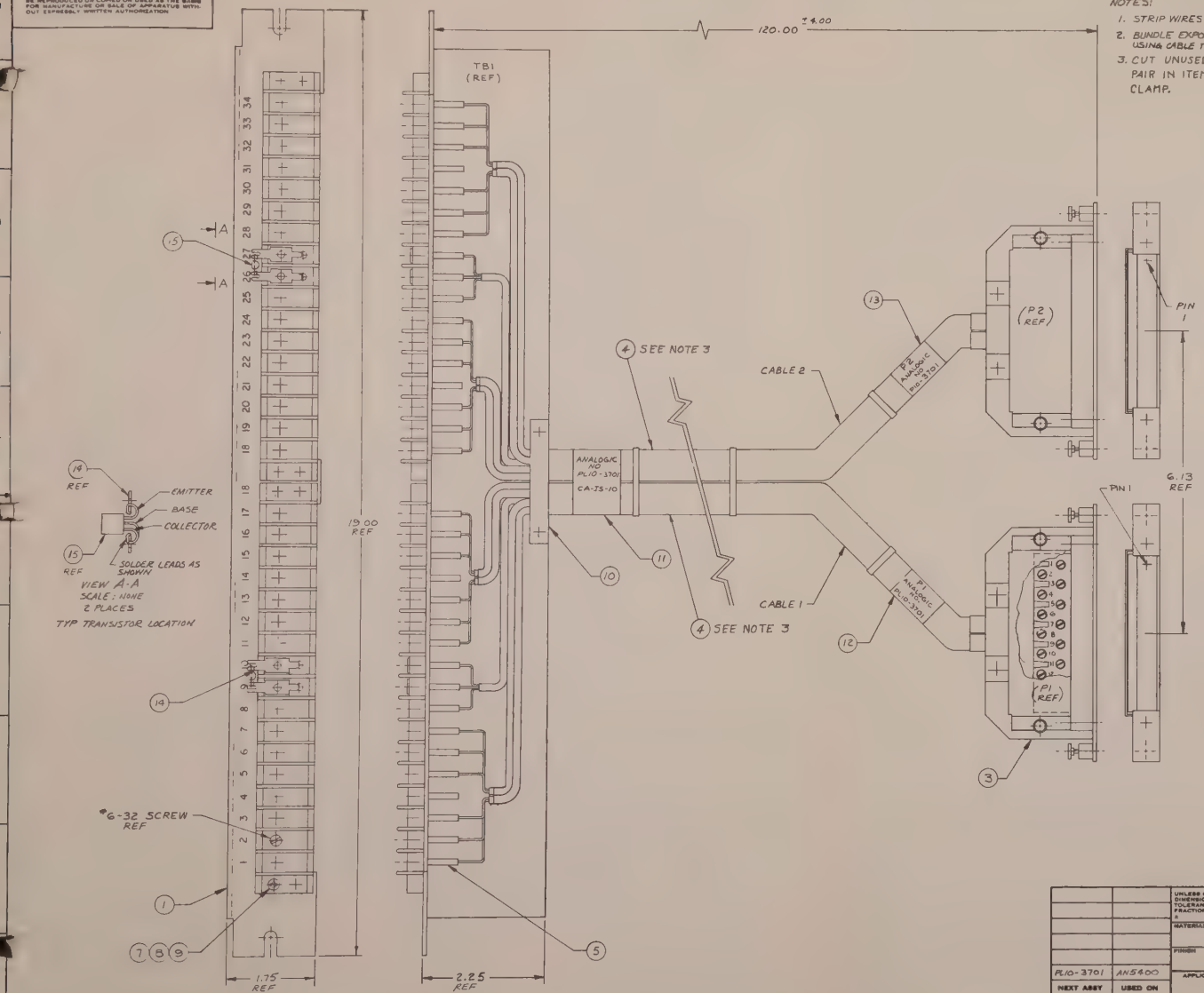
CAGE IDENT NO.	SIZE	DWG NO.	REV
31814	D	7-1581	2
SCALE 1/1	ACCOUNT NO.	SHEET 1 OF 1	

THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF ANALOGIC COMPANY AND SHALL NOT BE REPRODUCED OR COPIED OR USED AS THE BASIS FOR MANUFACTURE OR SALE OF APPARATUS WITHOUT EXPRESSLY WRITTEN AUTHORIZATION

NOTES:
1. STRIP WIRES .31±.03 BOTH ENDS
2. BUNDLE EXPOSED WIRES AND CABLES USING CABLE TIES AS REQ'D
3. CUT UNUSED TWISTED SHIELDED PAIR IN ITEM 4 BACK TO CABLE CLAMP.

REVISIONS

REV	ECO	DESCRIPTION	DWN	APP'D	DATE
1		CA-IS SECURE TRANSISTOR REMOVED FROM CONN - COLD JUNCTION SENSE ASSY'S ITEM 10	AC	[illegible]	[illegible]
2	A-0025	PER ECO	[illegible]	[illegible]	5-18-78
3	A-0086	PER ECO	[illegible]	[illegible]	7-14-78



WIRING TABLE

ITEM NO.	WIRE NO.	SIZE AWG	COLOR	FROM	TO	SIGNAL NAME	
CABLE 1 — 4	1 A		BRAID	TB1-1	P1-2	SHIELD Ø	CARD 1
	B	22	BLK	TB1-2	P1-1	LO Ø	
	C	22	RED	TB1-3	P1-3	HI Ø	
	2 A		BRAID	TB1-5	P1-5	SHIELD 1	
	B	22	BLK	TB1-6	P1-4	LO 1	
	C	22	RED	TB1-7	P1-6	HI 1	
	3 A		BRAID	TB1-8	P1-9	SHIELD COMP	
	B	22	RED	TB1-9	P1-8	HI COMP	
	C	22	BLK	TB1-10	P1-7	LO COMP	
	4 A		BRAID	TB1-11	P1-11	SHIELD 2	
	B	22	BLK	TB1-12	P1-10	LO 2	
	C	22	RED	TB1-13	P1-12	HI 2	
	5 A		BRAID	TB1-15	P1-14	SHIELD 3	
	B	22	BLK	TB1-16	P1-13	LO 3	
	C	22	RED	TB1-17	P1-15	HI 3	
CABLE 2 — 4	6 A		BRAID	TB1-18	P2-2	SHIELD Ø	CARD 2
	B	22	BLK	TB1-19	P2-1	LO Ø	
	C	22	RED	TB1-20	P2-3	HI Ø	
	7 A		BRAID	TB1-22	P2-5	SHIELD 1	
	B	22	BLK	TB1-23	P2-4	LO 1	
	C	22	RED	TB1-24	P2-6	HI 1	
	8 A		BRAID	TB1-25	P2-9	SHIELD COMP	
	B	22	RED	TB1-26	P2-8	HI COMP	
	C	22	BLK	TB1-27	P2-7	LO COMP	
	9 A		BRAID	TB1-28	P2-11	SHIELD 2	
	B	22	BLK	TB1-29	P2-10	LO 2	
	C	22	RED	TB1-30	P2-12	HI 2	
	10 A		BRAID	TB1-32	P2-14	SHIELD 3	
	B	22	BLK	TB1-33	P2-13	LO 3	
	C	22	RED	TB1-34	P2-15	HI 3	

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PL10-3701	AN5400		
NEXT ASSY	USED ON	APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON FRACTIONS DECIMALS ANGLES

MATERIAL

FINISH

APPLICABLE SPECIFICATIONS

DRAWN	N.W. CARTER	6-16-77
CHECKED	[illegible]	8-JUL-77
DESIGNER	[illegible]	8-28-77
ENGINEER	[illegible]	8-28-77
APPROVED	[illegible]	9-22-77
RELEASED	[illegible]	[illegible]
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

CABLE ASSEMBLY (CA-IS-10)

CODE IDENT NO	SIZE	DWG NO	REV
31814	D	7-2301	3

SCALE 1/1 | ACCOUNT NO | SHEET 1 OF 1

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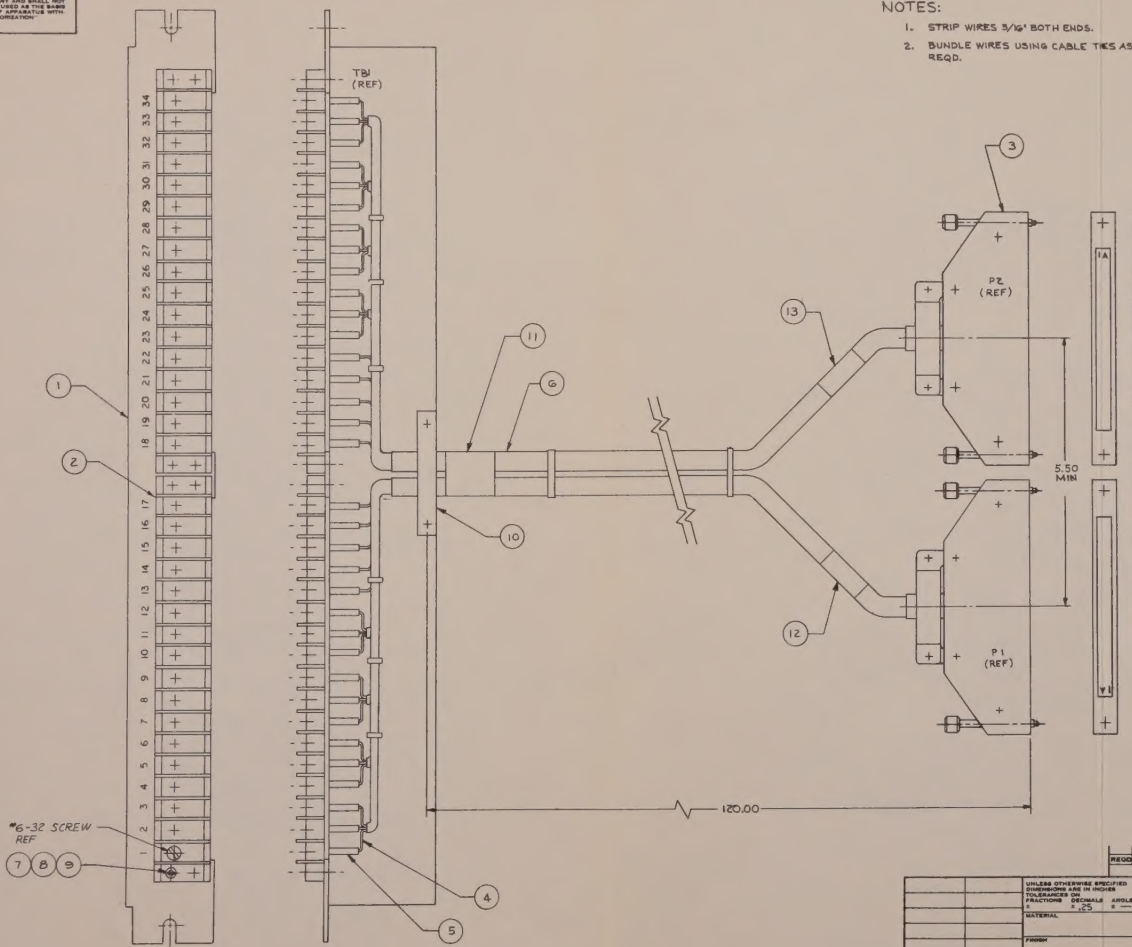
NOTES:

1. STRIP WIRES 5/16" BOTH ENDS.
2. BUNDLE WIRES USING CABLE TIES AS REQD.

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APP'D	DATE
1	A-8041	SEE E.C.O.	JDC	LMT	6-30-77
2	A-8088	SEE ECO	RSP	LMT	8-16-78

D 7-1583 A



WIRING TABLE

ITEM NO.	WIRE NO.	SIZE AWG	COLOR	FROM	TO	SIGNAL NAME	
4	1	24	WHITE	TBI-1	P1-D	IN Ø	CARD 1
	2			TBI-2	P1-E	RET Ø	
	3			TBI-3	P1-S		
	4			TBI-4	P1-J	IN 1	
	5			TBI-5	P1-K	RET 1	
	6			TBI-6	P1-9		
	7			TBI-7	P1-P	IN 2	
	8			TBI-8	P1-R	RET 2	
	9			TBI-9	P1-14		
	10			TBI-10	P1-U	IN 3	
	11			TBI-11	P1-V	RET 3	
	12			TBI-12	P1-18		
	13			TBI-13	P1-4		
	14			TBI-14	P1-6		
	15			TBI-15	P1-21	SIG RET	
	16			TBI-16	P1-Z	ANA GND	
	17			TBI-17	P1-1	ANA GND	
	18			TBI-18	P2-D	IN Ø	CARD 2
	19			TBI-19	P2-E	RET Ø	
	20			TBI-20	P2-S		
	21			TBI-21	P2-J	IN 1	
	22			TBI-22	P2-K	RET 1	
	23			TBI-23	P2-9		
	24			TBI-24	P2-P	IN 2	
	25			TBI-25	P2-R	RET 2	
	26			TBI-26	P2-14		
	27			TBI-27	P2-U	IN 3	
	28			TBI-28	P2-V	RET 3	
	29			TBI-29	P2-18		
	30			TBI-30	P2-4		
	31			TBI-31	P2-6		
	32			TBI-32	P2-21	SIG RET	
	33			TBI-33	P2-Z	ANA GND	
4	34	24	WHITE	TBI-34	P2-1	ANA GND	

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PL10-2159	AN5400		
NEXT ASSY	USED ON		
APPLICATION			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON FRACTIONS DECIMALS ANGLES ± .25 ± .—

MATERIAL

FINISH

APPLICABLE SPECIFICATIONS

WEIGHT

	DRAWN	DATE
	M.H. Carter	1/11/77
CONTROL		1/21/77
DESIGNER		1/26/77
ENGINEER		2-1-77
MFG		2-18-77
RELEASE		8/4/77

ANALOGIC WAKEFIELD, MASS. 01880

CABLE ASSEMBLY (CA-SHI-10)

WORK ORDER NO.	SIZE	DWG NO.	REV
31814	D	7-1583	B

SCALE 1/1 ACCOUNT NO. SHEET 1 OF 1